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PWM OF CASCADED MULTILEVEL VOLTAGE SOURCE INVERTER USING FIELD PROGRAMMABLE GATE ARRAY

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Abstract - Multilevel inverter finds its application in high voltage and high power converters. Various topologies of multilevel inverter provides several advantages including power voltage stress, higher efficiency, lower EMI, better waveform and improved THD. This paper presents the development of Altium FPGA as a control circuit for generation of the Digital Pulse Width Modulation (DPWM) signal for the single-phase cascaded H-bridge multilevel inverter. The FPGA chip is chosen for the hardware implementation due to its ability to produce accurate results at a high computational speed. Counter based Digital Pulse Width Modulation (DPWM) for increased resolution without unnecessarily increasing the clock frequency is used. In addition to Altium Nanoboard FPGA, Xilinx System Generator / MATLAB software has been used for simulation and verification of the proposed circuit before implementation. The simulation and experimental results are in close agreement.

Keywords – Cascaded H-Bridge (CHB), Multilevel Inverter (MLI), Digital Pulse Width Modulation (DPWM), Total Harmonic Distortion (THD), Field Programmable Gate Array (FPGA)

I.INTRODUCTION TO MULTILEVEL INVERTERS

There is growing interest for multilevel inverter(MLI) topologies since they extend the application of power electronics system to higher voltages and power ratio.MLI is the most attractive technology for the medium to high voltages range, which includes motor drives, power drives, power distribution, power quality and power conditioning applications.MLI includes an array of the power semiconductors devices and number of voltage sources, the output of which generates voltage with many levels. The communication of the switches permits the addition of the capacitor voltages which reaches high voltage at the output, while the power semiconductors must withstand only reduced voltages. Number of voltage sources from a single voltage source is obtained by clamping the voltage

at different level with the help of clamping capacitors. The most attractive features of MLI are as follows:

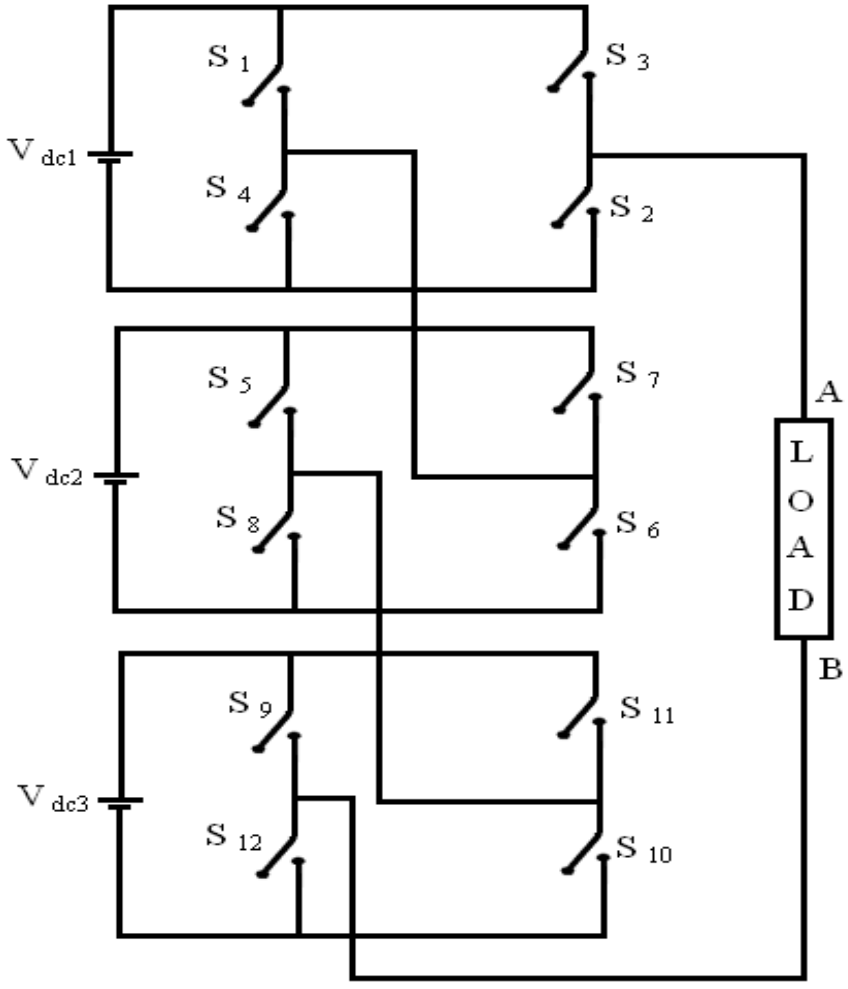
Generate output voltage with extremely low distortion and lower dv/dt Draw input current with very low distortion. Generate smaller common-mode (CM) voltage, thus reducing the voltage stress in the motor bearings. Ability to operate with a lower switching frequency. For High power applications, voltages and currents need to be pushed up. Semiconductor switch ratings have limited the applications of power converters rated in tens to hundreds of megawatts. Large inverters operating at these power levels require power devices at higher rating. Hence, maximum ratings of the power semiconductor have become a major problem. Even though switches with higher voltage rating are available, their cost is high. Series and/or paralleling of devices leads to higher current levels whereas series connection of switches provides higher voltage levels. Higher voltage level is achieved by replacing the switches in these inverters by series connection of devices with low voltage rating so that each individual switch shares the impressed DC link voltage with the others in the string during its turn off state. Connection of devices in series, achieving equal voltage sharing among the switches is a major problem. Multilevel topologies are based on the principle and therefore the voltages applied to the devices are controlled. One advantage of MLI compared with two-level topology is that, it produces more voltage levels. Hence, the output is ready is easily filtered with filtering components and also the switching frequencies of the devices is reduced. These two benefits reveal the use of MLI in high power applications. The main drawbacks of the MLI are as follows:

Several topologies require more number of switches and involves control complexity. Several DC voltage sources are required, which are usually provided by capacitors ,balancing the voltage of these capacitors according to an operating point is a significant challenge. Several topologies used in high voltage and high power application reveal that, they have been around for more than 25 years .An early traceable patent named R.H.Baker and L.H.Banniester introduced cascaded MLI in the year 1975 that connects separately dc-sourced full-bridge cells in series to synthesize a staircase ac output voltage. The advantage of this topology is that it does not require additional voltage source or capacitors, while the disadvantage is being requirement of several dc sources. A novel cascaded MLI using a single dc source was proposed by Z.Du, L.M.Tolbert, J.N.Chiasson and B.Ozpineci, which requires a single power source. Through the manipulation of the cascaded inverter with diodes blocking the sources, the diode-clamped MLI has been proposed by Nabae et al,in the year 1981 which eliminates the use of separate dc sources. The diode- clamped inverter was also called neutral-point clamped inverter when it was used in three level inverter in which the mid-voltage level was defined as the neutral-point and doubles the device voltage level. The Capacitor-clamped inverter is similar to the diode-clamped inverter which uses clamping capacitor instead of clamping diodes in their mode of operation. The advantage of this topology is that it does not require separate dc sources, while the disadvantage is that, it does not have balanced voltages. The above three configuration are widely used and all these configurations requires more number of switches to get the required level. A novel cascaded sources multilevel dc-link inverter with input sources cascaded (CSMLDCL) to an H-bridge inverter has been proposed by S,Jeevananthan et al, in the year 2003 which effectively reduces the number of components. More recently (2005), a new class of multilevel inverter was found by Gui-Jia, which was based on multilevel dc-link (MLDCL) and an H-bridge inverter. This MLDCL is a diode-clamped phase leg, flying capacitor phase leg and cascaded half bridge cells.

Comparison of Power Component Requirements Per Phase Leg Among Three Multilevel Inverters

Inverter Configuration	Diode Clamped	Flying Capacitors	Cascaded inverters
Main switching devices	2 (m–1)	2(m–1)	2(m–1)
Main diodes	2 (m–1)	2(m–1)	2(m–1)
Clamping diodes	(m–1) (m–2)	0	0
DC bus capacitors	(m – 1)	(m – 1)	(m – 1)/2
Balancing Capacitors	0	(m – 1) (m – 2)/2	0

In very high power application especially with very high input voltage, traditional two-level VSIs could not avoid to sue the series connected semiconductor switches so as to cope with limitations of device rating utilized and it may be very cumbersome and even problematic mainly due to difficulty of device matching deteriorating utilization factor of switching devices. The multilevel topology, however, suggests a good solution for such a problem.



Line Diagram of seven level MLI :

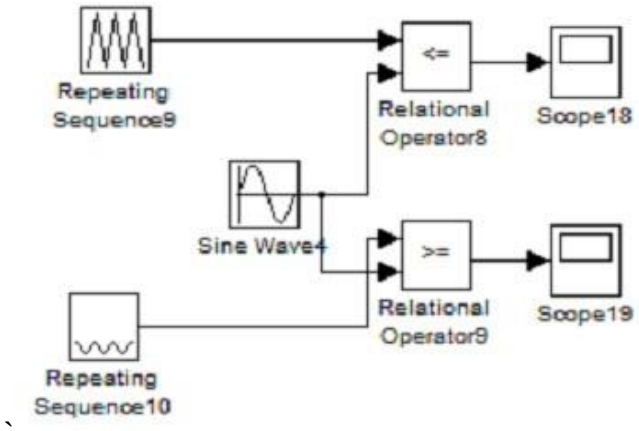
Modes of Operation:

The operation of the MLI involves seven output levels namely level 1 to level 7. Each level contributes to a voltage level and the overall output voltage is given by adding the magnitude of the levels.

12	Mode	S1	S2	S3	S5	S6	S7	S8
Vdc1+Vdc2+ Vdc3	1	1	0	0	1	0	1	0
Vdc1+Vdc2	2	0	1	0	1	1	1	0
Vdc1	3	0	1	1	1	0	1	0
0	4	0	0	0	0	0	0	0
-Vdc1	5	0	1	1	1	0	0	1
-Vdc1-Vdc2	6	0	1	0	1	1	0	1
-Vdc1-Vdc2-Vdc3	7	1	0	0	1	0	0	1

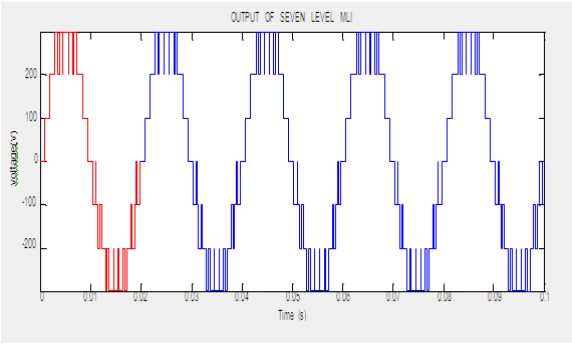
Circuit diagram for generating PWM

The circuit for the generation of PWM signals by Sub harmonic PWM method for one level of cascaded multilevel inverter.

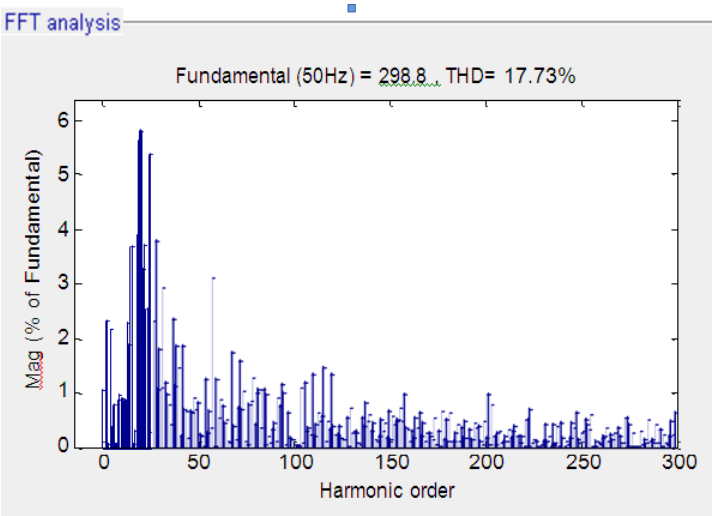


Output Waveform of seven level inverter:

The output voltage waveform for the proposed topology with PWM technique is shown in the figure. The voltage waveform has seven levels with each level contributing 100v and output is obtained across the resistive load of 100 ohms.

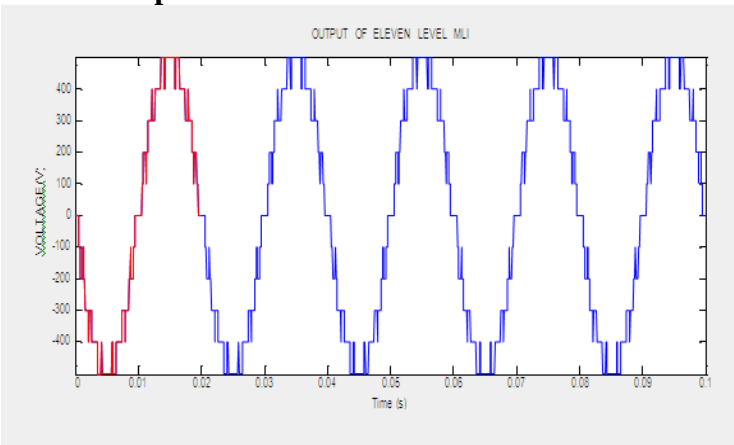


Total harmonic distortion of Seven Level Inverter

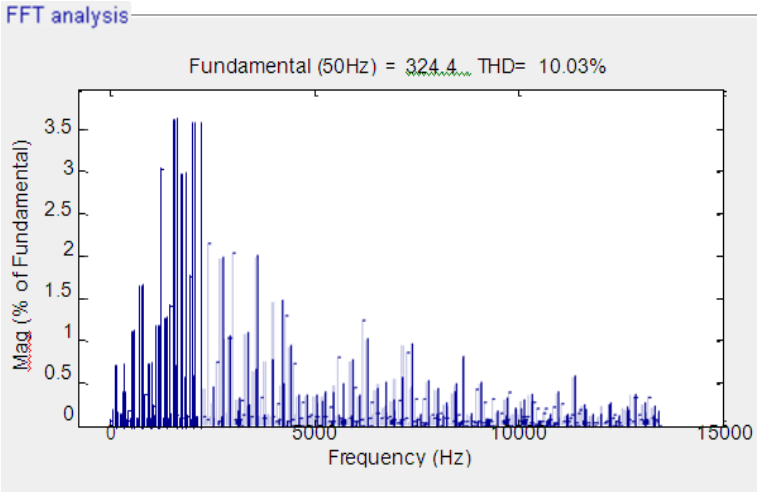


The above diagram shows the fast fourier transform analysis of the seven level MLI output. The total harmonic distortion was obtained to be 17.73% and the fundamental peak voltage was obtained as 299 volts at a frequency of 50 Hz.

Output waveform of Eleven Level MLI

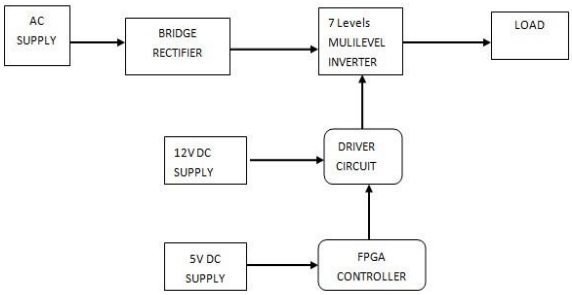


Total harmonic distortion of Eleven Level Inverter



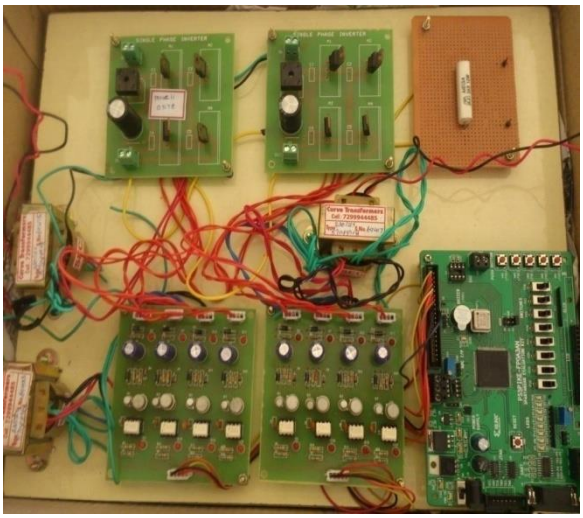
The above figure shows the Fast Fourier Transform Analysis of the eleven level MLI output. The total harmonic distortion is obtained to be 10.03% and the fundamental peak voltage is found to be 324.4 V at a frequency of 50Hz.

Block diagram of Hardware



The above diagram shows the block diagram of the cascaded H-Bridge inverter. In this the AC supply is converted to DC using Bridge Rectifier which is the input to the MLI. The controller used to control the switches of MLI is FPGA controller. Since the signal strength of FPGA controller is not enough to switch ON the switches of the inverter. Hence we use a driver circuit in order to amplify the signal of the FPGA controller so as to drive the switches of MLI. The supply voltage for the driver circuit is given from the rectified output of the step down transformer. The input to the FPGA controller is given using a regulator.

Hardware Setup



The hardware setup for seven level single phase cascaded H-bridge MLI is shown in figure. The hardware setup consists of single phase uncontrolled rectifier, FPGA controller, driver circuit and multilevel inverter. Cascaded multilevel inverters synthesize a medium voltage output based on a series connection of power cells which use standard low-voltage component configurations. This characteristic allows one to achieve high-quality output voltages and input currents and also outstanding availability due to their intrinsic component redundancy. The cascaded multilevel inverter has been recognized as an important alternative in the medium-voltage inverter market

FPGA

FPGAs are "fine-grain" devices. That means that they contain a lot (up to100000) of tiny blocks of logic with flip-flops. FPGAs are RAM based. They need to be "downloaded" (configured) at each power-up. FPGAs have special routing resources to implement efficiently binary counters and arithmetic functions (adders, comparators...) and RAM. FPGAs can contain very large digital designs, while CPLDs can contain small designs only.

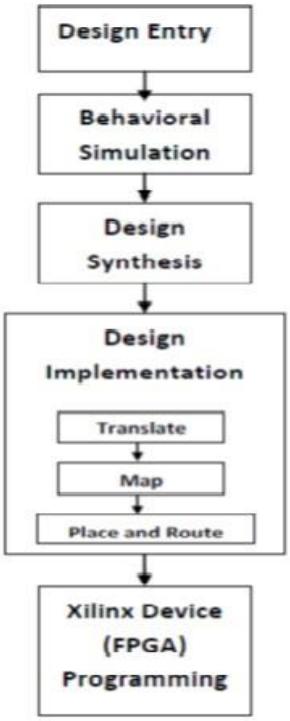
Design Procedure on FPGA

The Field Programmable Gate Array (FPGA) ,as the name suggest, is a array of logic cells (or modules) and interconnects, which can be reprogrammed depending upon the requirement of the user. We can design it and make changes in it whenever required. It provides instant manufacturing turnaround and negligible prototype costs which makes it suitable for embedded system design.

Design Entry

This is the first step of implementing a design on FPGA. In this step the VHDL (Very High Speed Integrated Chip Hardware Description Language) code of PWM Generator Architecture was written using software Xilinx ISE 10.1. Structural modeling was used for writing the code. After writing the code syntax check was performed on the code to see whether code was properly written using correct syntax

FPGA Design Flow



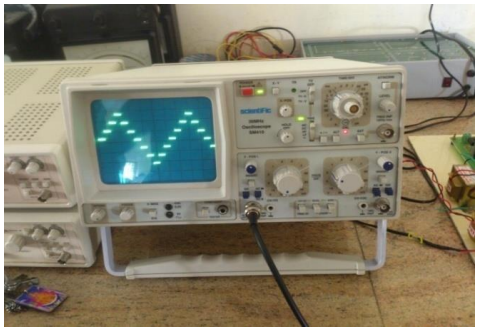
Advantages of FPGA based design

Field Programmable Gate Array (FPGA) offers the most preferred way of designing PWM Generator for Power Converter Applications. They are basically interconnection between different logic blocks.

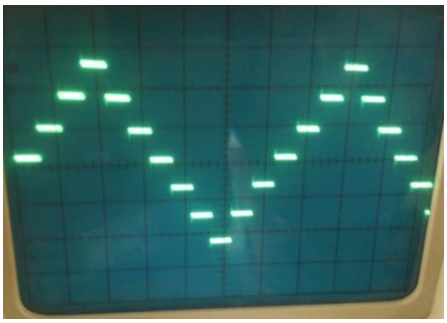
When design is implemented on FPGA they are designed in such a way that they can be easily modified if any need arise in future. We have to just change the interconnection between these logic blocks. This feature of Reprogramming capability of FPGA makes it suitable to make your design using FPGA . Also using FPGA we can implement design within a short time. Thus FPGA is the best way of designing digital PWM Generators. Also implementation of FPGA-based digital control schemes prove less costly and hence they are economically suitable for small designs .Hence in this thesis FPGA based PWM Generator technique is discussed.

Hardware Result

A prototype of single phase MLI is constructed/fabricated using the parameter listed in simulation. The output of the hardware is shown in the figure



Seven level output waveform



Comparison between Seven Level and Eleven Level MLI

The THD of Seven Level Inverter was found to be 17.73% and that of eleven level inverter was found to be 10.03%.The difference in the THDs between the two MLIs shows that the increase in level increases the efficiency of the MLI. But increasing the number of switches in order to increase the number of levels will cause increase in switching losses and harmonics. Hence, we need to obtain a compensation between the two.

CONCLUSION

We hereby conclude that Multi-level inverters is a very promising technology in the power industry. In this project, a new inverter topology has been implemented which has superior features over conventional topologies in terms of the required power switches, control requirement's, cost and

reliability. PWM Generator architecture which was downloaded onto FPGA can be used to control Gate signal of Power Switches of Inverter. By this way we can be able to control ON and OFF time of Inverter. Hence we can use this architecture for controlling Inverter which produces AC from DC source. Hence PWM Inverter is implemented using FPGA based PWM Generator. A single phase Cascade H-Bridge Inverter is designed and implemented practically. The components used in the practical implementation of H-Bridge Inverter are described in detail.

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