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DESIGN OF LOW POWER 8T & 10T SRAM

C.Siva Sankari, S.Ramya, C.Iswarya, K.Sripriya, Kovilvenni
Electronic and Communication Engineering, Anjalai Ammal Mahalingam Engineering College,
K.Sathiya Bharathi
Assistant Professor, ECE Dept, Anjalai Ammal Mahalingam Engineering College,
Kovilvenni. Sathiya2188@gmail.com

Abstract **—** In this paper VDD pre-charge and charge recycling technique for low power read operation in 8T&10T SRAM cell was proposed. A 4T read port is designed to employ the proposed technique. Read BL (RBL) is charged and discharged through the read port according to the state of stored bit. Read port is powered by virtual power rails that run horizontal and are shared by the cells of a word. The dynamic control of read port power rails reduces the RBL leakage substantially.To overcome the bottleneck of 6T SRAM cell in terms of low voltage operation. Design a single 8T & 10T SRAM cell with following characteristics like Ultra Low Voltage operation, Low power consumption, Increased Write and Read Margin.

Index terms—SRAM, 6T, 8T, 10T, Low power, read and write operation.

I. INTRODUCTION

SRAM is mainly used for the cache memory in Microprocessors, mainframe computers, engineering workstations and memory in hand held devices due to High speed and low power consumption. The need for low-power design is becoming a major issue in high-performance digital systems such as microprocessors [1], Digital Signal Processors (DSPs) and other applications. The increasing Market of mobile devices and battery powered portable electronic systems is creating demands for chips that consume the smallest possible amount of power. SRAM consist of almost 60% of Very Large Scale Integrated (VLSI) circuits. It is also said that memories are the biggest culprit for the power dissipation in any digital system and No digital system gets complete without memories. Several techniques have been proposed to reduce the power consumption during Write operation of SRAM like, Segmented Virtual Ground Architecture for Low-Power Embedded SRAM [2], Low power SRAM design using half-swing pulse mode techniques [3] and A single-bit line cross-point cell activation (SCPA) architecture for ultra-low power SRAM's[4].Some other techniques which are used for low power SRAM like Half-Swing Pulse-Mode Techniques[5] these techniques are used for reduce the power dissipation of the SRAM circuit. All these discussed papers are used extra circuitry for reducing the power consumption. In this paper optimized SRAM cell contains two extra tail transistors in the pull-down path of the respective inverter to avoid charging of the bit-lines. These two trail transistor are controlled by an extra signal write select (WS). SRAM or Static random Access memory is a form of semiconductor memory widely used in electronics, microprocessor and general computing applications. This form of semiconductor memory gains its name from the fact that data is held in there in a static fashion, and does not need to be dynamically updated as in the case of DRAM memory. While the data in the SRAM memory does not need to be refreshed dynamically, it is still volatile, meaning that when the power is removed from the memory device, the data is not held, and will disappear. There are two key features to SRAM - Static random Access Memory, and these set it out against other types of memory that are available: The data is held statically: This means that the data is held in the semiconductor memory without the need to be refreshed as long as the power is applied to the memory. SRAM is a form of random access memory: A random access memory is one in which the locations in the semiconductor memory can be written to or read from in any order, regardless of the last memory location that was accessed. Fig 1 shows the read/write operations of an SRAM. To select a cell, the two access transistors must be "on" so the elementary cell (the flip-flop) can be connected to the internal SRAM circuitry.

II. EXISTING SYSTEM

Conventional 6T SRAM cell consists of six transistors. Figure shows the conventional 6T SRAM cell. Transistors N2 and N3 are access transistor, while remaining four transistors: N1, N2, P1 and P2 form two inverters. These two inverters are used to latch data. The data enters into latching inverter through access transistor. The process of introducing a data is known as write operation and retrieving a data is known as read operation. Word line (WL) selects a row of SRAM cell. Bit line (BL) and bit line bar (BLB) are used to select a column of SRAM cell. When both WL and BL are ON, a particular SRAM cell is selected.

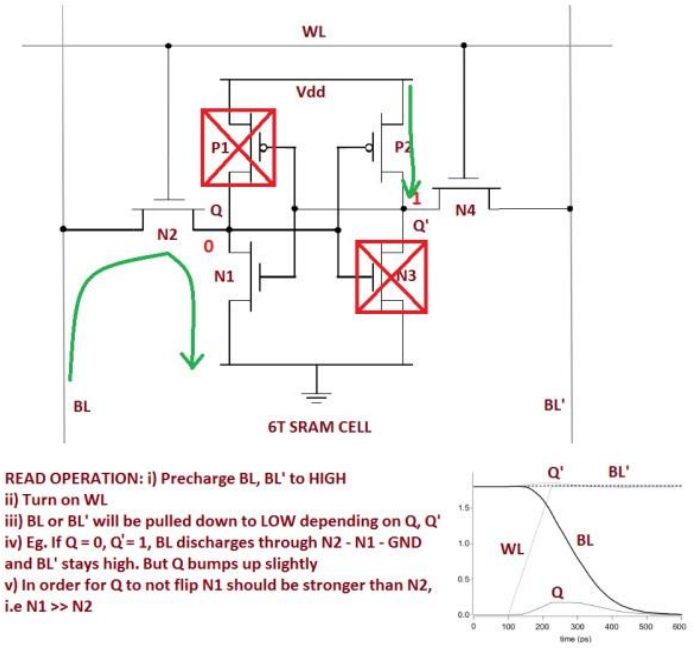

Figure.1.6T SRAM Cell Read Operation.

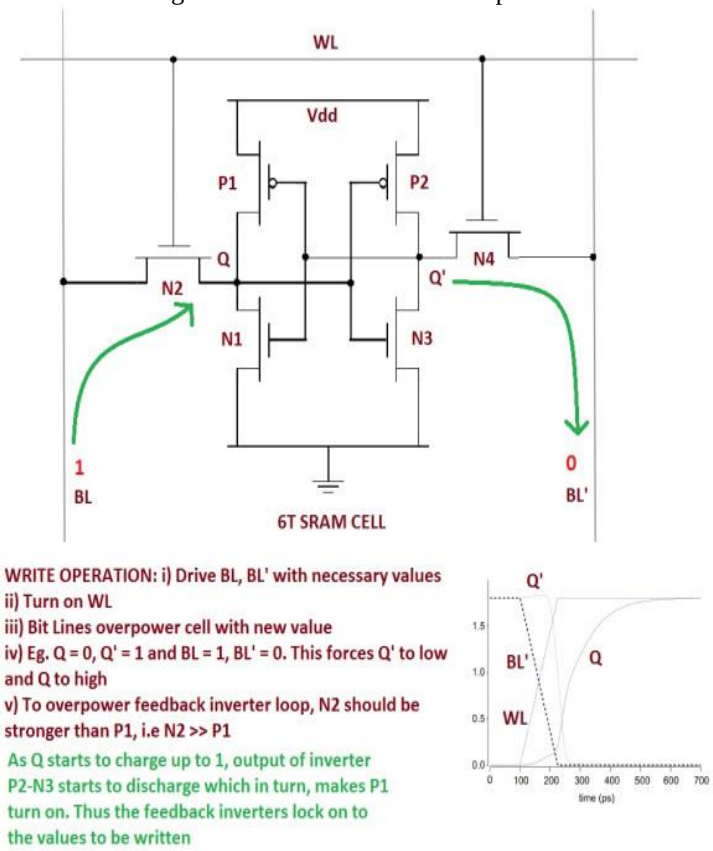

Figure.2.6T SRAM Cell Write Operation.

III. PROPOSED WORK

The architecture of an 8T & 10T SRAM cell is similar to the 6T SRAM cell except additional read circuitry. Figure shows the designed 8T & 10T SRAM cell. In this 8T & 10T SRAM cell, 10 transistors have been used. It consists of conventional 6T SRAM cell and an additional read circuitry. Difficulty in conventional 6T SRAM cell is the high risk of data loss during read operations. There is possibility of flipping node voltage at Q and Q' due to back to back inverter actions. This situation can be avoided using extra read circuitry. In this 8T & 10T SRAM cell, write operation is same as in 6T SRAM cell. In case of read operation, charge sharing takes place between read bit line (RBL) and uncharged bit line BL / BLB during read operation. Due to sharing of charge, read bit line does not discharge completely and stay at mid voltage level. Hence this cell behaves as an automatic bit line swing limits.

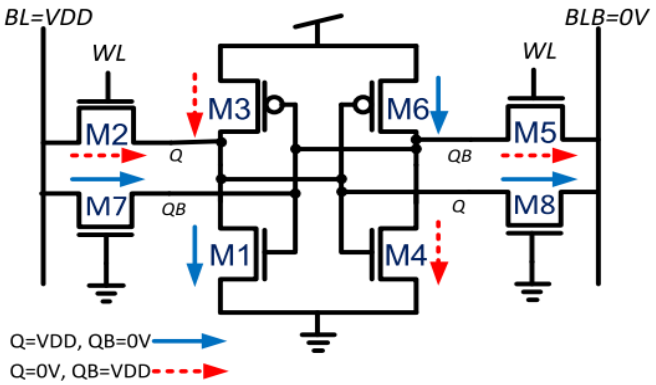

Figure.3.8T SRAM Cell.

The previous INV+TG-based 8T & 10T cell was application specific, while our proposed design is generic. Have used the dynamically controlled power rails for the read port. Pre-charge RBL at VDD/2, while the previous 8T & 10T design eliminated the pre-charge phase, and used INV to fully charge or discharge the RBL. The basic read technique of both the designs is completely different. The main idea of the proposed design is "the charging or the discharging of the read BL from VDD/2 for every read operation." The previous design either discharges from VDD to VSS, or charges from VSS to VDD. A powerful INV was used previously to produce full VDD swing on the RBL. In the proposed design, RBL is precharged at VDD/2, and only a small voltage difference (comparable with 6T) is produced for every read cycle. In the proposed design, for every read cycle the RBL will exhibit some change (positive or negative) from its precharged value of vdd/2.

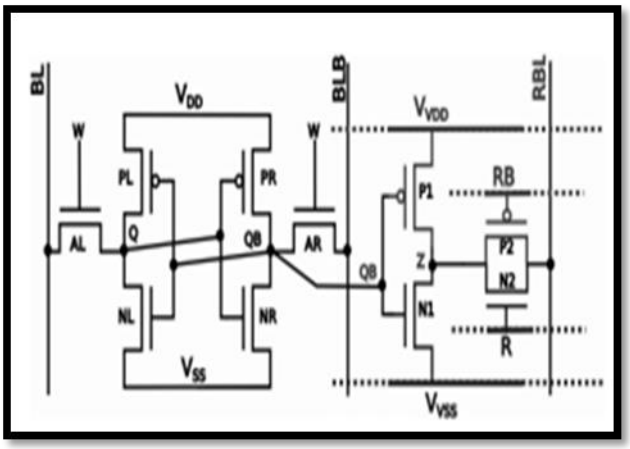

Figure.4.10T SRAM Cell.

IV.FUTURE WORK

FinFET technology has recently seen a major increase in adoption for use within integrated circuits. Compared to the more usual planar technology, FinFET transistor technology offers some significant advantages in IC design. The FinFET technology promises to provide the deliver superior levels of scalability needed to ensure that the current progress with increased levels of integration within integrated circuits can be maintained. The FinFET offers many advantages in terms of IC processing that mean that it has been adopted as a major way forwards for incorporation within IC technology.

V. SOFTWARE USED

Tanner EDA by Mentor Graphics now enjoys the stability that comes with joining a successful big 3 EDA company. Mentor will continue to invest in the Tanner EDA suite to strengthen it as the user base and support Tanner EDA products, their customers and their foundry partners and place particular focus on IoT users who design and integrate: power electronics, sensors, MEMS, photonics and RF circuitry. Tanner EDA solutions by Mentor Graphics provides a complete line of EDA software tools that drive innovation for the design, layout, and verification to tape-out of analog and digital integrated circuits (ICs). Tanner EDA solutions offer a complete design environment supporting analog, mixed-signal, or MEMS domains in one highly-integrated end-to-end flow. Our customers are creating breakthrough applications in areas such as Automotive, Life Sciences, imaging, sensors, power management, Military, Aerospace, Space, Internet of Things (IoT) and ARM Powered solutions. Tanner EDA products have a low learning curve, high interoperability, and a powerful user interface improve design team productivity.

VI. CONCLUSION

The 8T & 10T SRAM cell is designed in CMOS technology and its performance characteristic has been analysed. The designed 8T & 10T SRAM has write capability as good as 6T SRAM and improved read stability than 6T SRAM cell. The power dissipation, delay, and power delay product of the designed 8T & 10T SRAM cell.

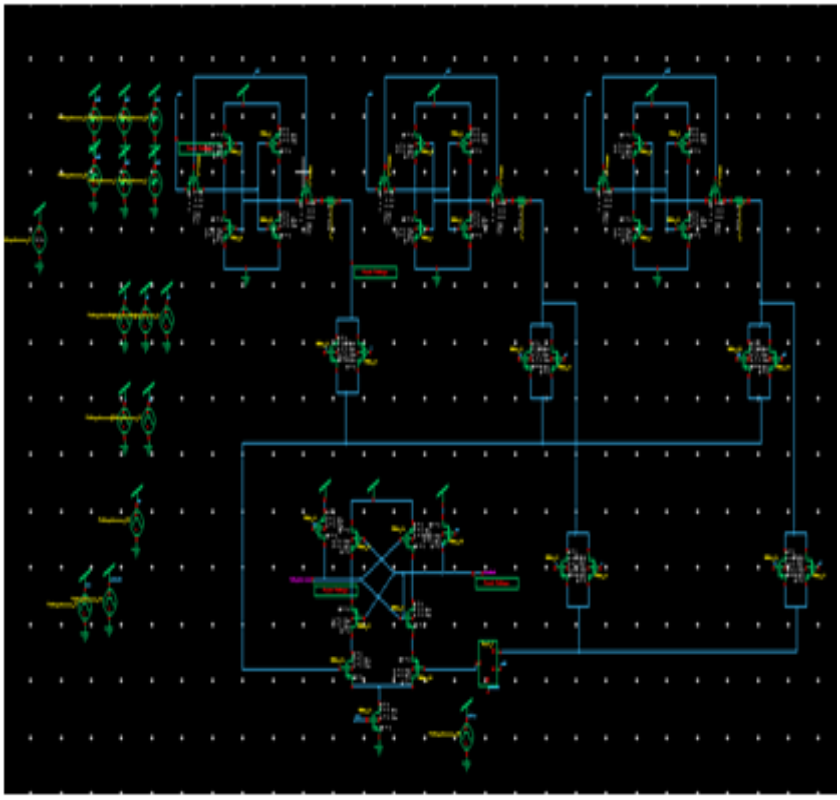

Figure.5.8T SRAM Cell Tanner Schematic Diagram.

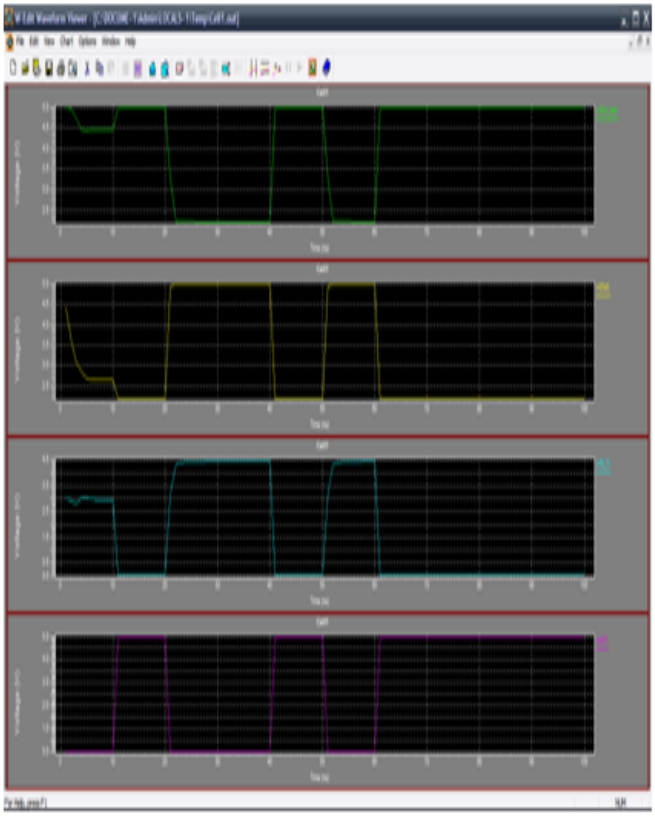

Figure.6.Tanner Tool Result.

In this paper we focus on the dynamic power dissipation during the Write operation in CMOS SRAM cell. The charging and discharging of bit lines consume more power during the Write ―1‖ and Write ―0‖ operation. 8T SRAM cell includes two more trail transistors in the pull down path for proper charging and discharging the bit lines. The results of 8T

SRAM cell are taken on different frequencies at power supply of 1.5 V. The circuit is characterized by using the 130 nm technology which is having supply voltage of 1.5 V. Finally the results are compared with Conventional 6T SRAM cell. The power dissipated in low power 8T SRAM cell is reduced in comparison to conventional 6T SRAM cell. The result of the research has practical reference value for further study.

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