International Journal on Recent Researches in Science, Engineering & Technology (IJRRSET)
A Journal Established in early 2000 as National journal and upgraded to International journal in 2013 and is in existence for the last 10 years. It is run by Retired Professors from NIT, Trichy. Journal Indexed in JIR, DIIF and SJIF.
Research Paper
Available online at: www.jrrset.com

ISSN (Print) : 2347-6729
ISSN (Online) : 2348-3105
Volume 7, Issue 2
February 2019.
JIR IF : 2.54
SJIF IF : 4.334
Cosmos: 5.395

Received on: 05.01.2019 Published on: 28.02.2019 Pages : 49 - 54

DESIGN OF LOW POWER MIXED SIGNAL CMOS PROGRAMMABLE GAIN AMPLIFIER FOR HEARING AIDS

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Abstract

With the continuous advancement of standards in telecommunication systems, requirements for analog circuitry will become ever more demanding. The newer standards not only utilize better modulation schemes, demanding less noise with higher linearity, but also require increased bandwidth from analog circuitry. This paper describes a fully differential, common mode feedback compensated Programmable Gain Amplifier with operational trans-conductance amplifier capable of providing a gain of 84 dB and consumes low power of <124µW. The proposed PGA has been fabricated in SMIC 28nm CMOS process. They are implemented in CMOS technology as the gain varies in Trans-conductance amplifier remains relatively invariable around 1GHz.
Keywords: Programmable Gain Amplifier, Operational Trans-conductance Amplifier, common mode feedback amplifier, CMOS, mixed signal, hearing aid

Introduction

With the rapid progress of society and great change in the way of life, people pour more and more attention into their own health. According to the WHO No. 300th report in 2014, there are more than 360 million people with hearing loss in the world. Among these people, more than 90% of them can compensate their hearing loss by wearing a hearing aid device to achieve the basic functions of the hearing. As the core of hearing aid device, v (SoC). And it is extremely difficult to satisfy the high dynamic range, low noise, low power consumption and configuration requirements with all functions integrated in a single chip. Digital hearing aid SoCs in reference [1, 2] mainly focuses on hearing aid algorithm realization. Reference [3, 4] are analog hearing aid chips and don't realize any configured noise reduction algorithm. Reference [5] is an implementation of mixed signal SoC design with basic hearing compensation using subthreshold transistor design technique. With low power consumption, the chip guarantees the enough dynamic range of output signal. But because the subthreshold technique is affected much by process parameter influence, the chip is not suitable for mass production of industrialization. Since there is still no complete-function hearing aid SoC for practical application, this paper presents a low power, high performance and flexible mixed-signal PGA, which covers all the critical features of today's hearing aids chip.

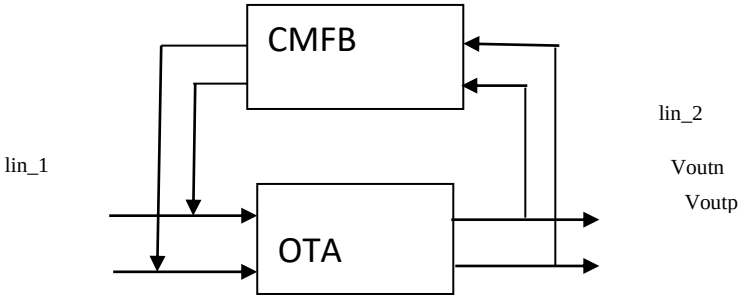


Fig.1. Basic Block Diagram of CA-TIA

The PGA circuit is shown as Fig.2. Two common-mode voltage generators are composed of the resistor divider from power supply to ground, providing 0.5V common-mode voltage for differential transconductance amplifier (OTA). Onboard capacitors C1 and C2 are used to reduce power supply high-frequency noise and ripple for the differential inputs.OTA and switching resistance array can realize adjustable gain range of -6dB to 30dB in 3dB step continuously under the control of DSP.The gain of the PGA is given by:

$$A = 2^{\frac{n-1}{gain\_cntr}}$$

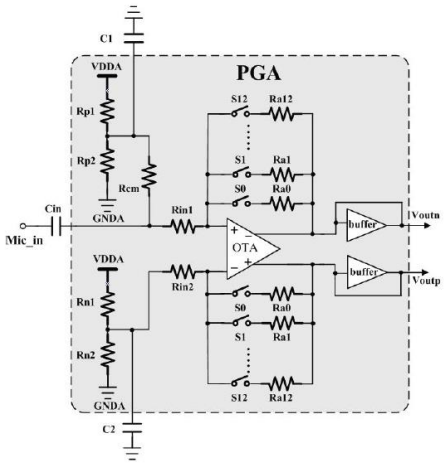


Fig.2 Block diagram of PGA

A detail schematic of OTA in PGA is shown in Fig.3,which adopts differential two-stage Class-AB Nested-Miller compensation structure with main OTA and common-mode feedback (CMFB) amplifier. The main feature of two-stage OTA is that it has less noise with high gain and large output swing. The load transistors of the first stage are split into two halves, the first ones (NM1a、NM2a) are biased by a constant voltage Vbias and the second ones (NM1b 、NM2b) are driven by CMFB amplifier. This solution reduces the load capacitance at the CMFB output and also improves OTA loop stability.

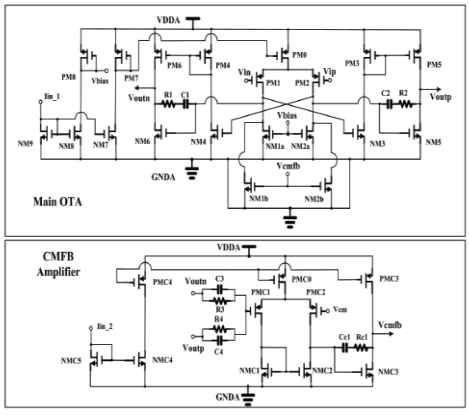


Fig.3 OTA circuit of PGA

By using PMOS input differential pair, the 1/f noise is reduced and the common-mode input level can be lower. In the second stage, PM3/ NM3, PM5/ NM5 and PM4/ NM4, PM6/ NM6 form the Class-AB output stage to save quiescent current and realize the rail-to-rail output swing. In CMFB circuit design traditional two-stage OTA needs two CMFB amplifiers to bias the first and second stage respectively, which means CMFB amplifiers will consume much power in design. And since the open loop gain of single stage CMFB amplifier is limited, it cannot provide stable CMFB signal when OTA inputs audio signal of large amplitude. This paper presents a two-stage CMFB amplifier to complete the full OTA design. By power optimizing the CMFB amplifier is also a two-stage Nested-Miller compensated amplifier. The OTA demonstrates 84dB gain, 29MHz GBW, 59o phase margin for 2pF load, and consumes <124 μW power

CIRCUIT DESIGN

The designed amplifier has an operational trans-conductance amplifier which adopts differential two stage class AB nested-Miller compensation structure and a common mode feedback amplifier. The common mode feedback structure is used to have a sufficiently high loop gain in the whole desired operating BW. The nested Miller compensation

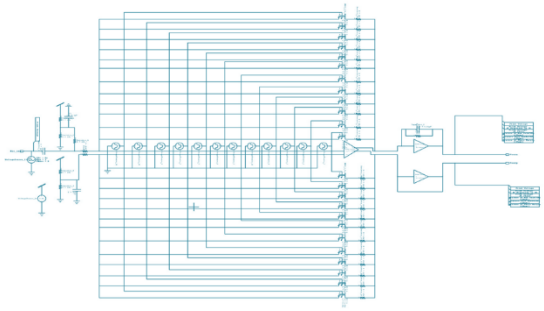


Fig4.represents the simulated circuit of PGA. Two common-mode voltage generators are composed of the resistor divider from power supply to ground, providing 0.5V common-mode voltage for differential trans-conductance amplifier (OTA). On board capacitors C1 and C2 are used to reduce power supply high-frequency noise and ripple for the differential inputs. OTA and switching resistance array can realize adjustable gain range of -6dB to 30dB in 3dB step continuously.

For the OTA, employing a feedback network consist of the parallel R_F and C_F as shown in fig 5.

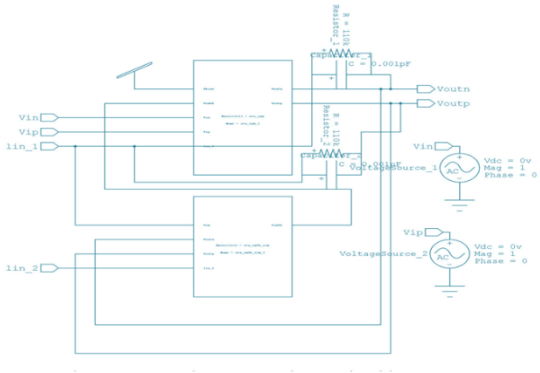


Fig.5. OTA Circuit Mode

A operational trans-conductance amplifier is the core of the proposed architecture. In differential architecture, it is greatly reduced as the coupling is determined by the mismatches between two nominally identical paths. In Differential OTA structure, the load resistances in amplifiers are implemented using MOS devices.

Active loading is used in applications where the required voltage gain of the amplifier is large. Active loads make use of the output impedance of the MOS devices which is higher than a poly resistor of the same dimensions. This maximizes the output impedance hence the voltage gain of the amplifier is accomplished using less silicon area than poly silicon resistors. Also, in case of resistively loaded amplifier the designer cannot set the operating current, gain and the common mode level independently from one another. In active it is possible to set the load impedance and current independently through physical device dimension and the common mode is determined by an external feedback loop. This adds flexibility to the design process. This design incorporates an actively loaded differential common-mode stage to prevent the feedback resistor from loading the differential common-mode input stage. Source follower has the characteristics of high input impedance and moderate output impedance.

The design of op-amps with good performance to power ratios often require a paradigm change, because on one hand, gain over the whole signal bandwidth is needed to have good linearity, but on the other hand lower UGF is wanted, to save the power used, because of the placement of non-dominant poles. The UGF in a large part determines the power consumption of the op-amp, because the non-dominant poles have to be designed with margin and pushed to higher frequencies. These two aspects of efficient design could be seen as an oxymoron. Even worse, the location of the UGF changes with the gain and equalizer configurations of the PGA. The biggest intrinsic challenge of the design is to hit the UGF perfectly in all conditions and place the zeros just in front of it, no matter the configuration of the PGA itself.

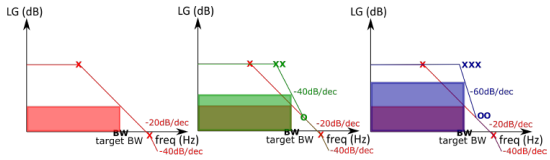


Fig. 6. Potential performance of a similar GBW amplifiers a) single pole b) dual pole and c) triple pole systems

This design strategy will lead to a clearly defined phase margin of around 60 degrees with a perfectly safe first-order roll off before the UGF (Fig 6a). To get the maximum performance obtainable, one should push the in-band poles just around band edge, to get the maximum loop gain in-band and leave them uncompensated until just before the UGF, where as many zeros as available should be placed to regain the lost phase (Fig. 6b, 6c).

SPICE SIMULATION AND VERIFICATION

The PGA is designed in 28nm CMOS technology with 0.5V supply voltage. NMOS and PMOS transistors are used for high frequency operation. The whole system is characterized in TANNER EDA SOFTWARE TOOL.

TANNER EDA provides a complete line software solution that catalyzes innovation for the design, layout and verification of analog and mixed signal integrated circuits. A low learning curve high interoperability and a powerful user interface improved design team productivity and enable a low total cost of ownership. It provides the powerful and most flexible Schematic Tool (S-Edit) that is available in the market.

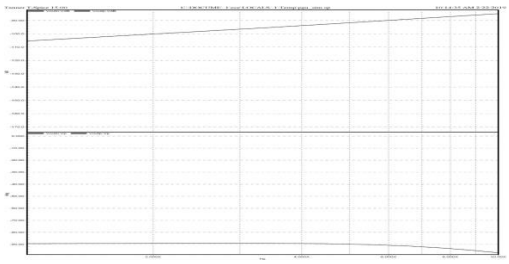


Fig.7.a). Post-Simulated Characteristic of PGA.

Spice Simulation characteristic of PGA are shown in the fig.7 a) and fig. 7.b)

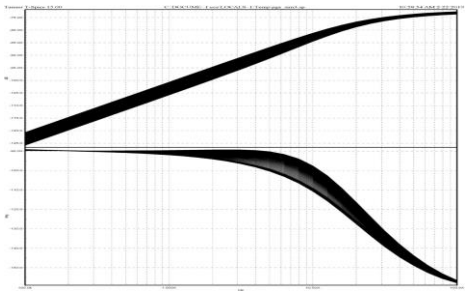
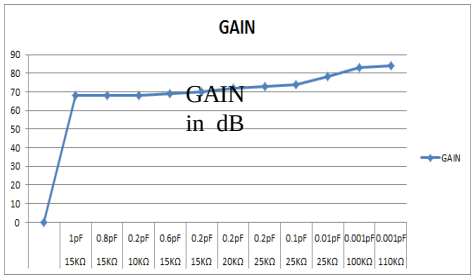


Fig.7.b). Temperature Analysis of PGA.

In this design with the feedback, Variable gain can be achieved by varying the resistance with constant bandwidth.



RESISTANCE (Ω) & CAPACITANCE (F)

Fig.8. Measured Differential Trans-conductance Gain of the PGA

From fig.8, the gain of the PGA varies accordingly with increase in the resistance and a decreased capacitance.

The layout diagram of the amplifier is shown in the fig. and the simulated frequency response is shown in fig.9

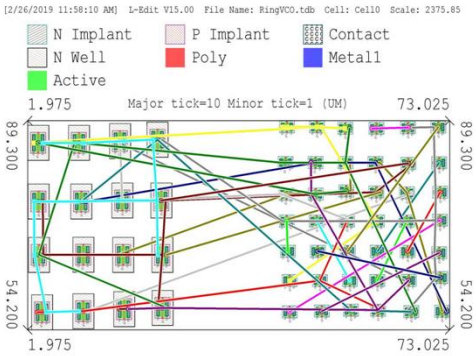


Fig.8. Simulated Layout of Differential OTA.

The layout challenge in OTA stage is the placement of the large feedback resistors so in this we use the resistor value of 90kΩ to 110kΩ.This issues relating to the layout of each of the components of the system are placement sizing and symmetry of the devices and it is very important for achieving the desired performance of the circuit. In order to minimize gate resistance and at the same time optimize noise performance, finger structures were used in each device in the design. Also the isolation of digital and analog sub-circuits was achieved through the use of guard ring structures which are also important for noise rejection.

The noise behavior of the added cross coupled pair in the stage is like a normal CG transistor and is neglected when the MOS channel length modulation effect is ignored.

Table list the measured performance summary. TABLE-I

PARAMETERS	[4]A-SSCC	[1]QR	[5]IMCAS	This work
TECHNOLOGY	0.13µm CMOS	28nm CMOS	0.13µm CMOS	28nm CMOS
FUNCTION	PGA [differential]	Class AB amplifier	PGA [OTA]	PGA [OTA with CMFB amplifier]
STAGE	3 stage	3 stage	2 stage	2 stage
GAIN	40 dB	70dB	82dB	84dB
POWER	285µW	<200µW	124µW	<124µW

Table I – Measured Performance Summary

CONCLUSION

Table I compares our work with previous works. This allows to have very high loop gain at signal BW without having to push the UGF into extreme frequencies, what in return allows to save power by not having to design many stages with non-dominant poles. To cover a large gain range, the PGA has been designed to have an internally configurable compensation. Measurements show a good correlation with simulations, especially with high gains, where excellent noise performance makes it possible for the ADC to capture even low power signals over long loops.

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