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Design and Implementation of a High-Density Standard Cell Library in UMC 180nm Technology.

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Abstract— Producing designs based on different technology at competitive cost has always been challenges to manufacturers. Some of the driving factors including portability, mobility, accuracy and increased performance demands. This brings the manufacturers to adapt certain methods such as decrease com- ponent sizes, increase its performance simultaneously, improve heat tolerance materials and etc. To design every logic gate at different driver strength will be time consuming. This paper provides solution for the above said challenges by developing our own standard cell for the given application. So, this can ensure us about the ability of precharacterised, preverified cells for utility in designing complex circuits. In high density standard cell library, the main objective is to increase density of logic cells that satisfies the given specifications. The benefit of high density cell library is used in devices where high computational speed or performance is not the constraint which leads to reduction in the space occupied by the devices.

Key Words: DSM (Deep Submicron Technology), SL (Standard Load), DRC (Design Rule Check), TT (Typical- Typical), SS(Slow-Slow), FF(Fast-Fast).

I. INTRODUCTION

IC development is nowadays a huge industry. There is an al- most infinite amount of consumer products like mobile phones, processors, televisions, cameras, refrigerators, ovens and cars that in one way or another uses custom IC components. For designing these components one approach is the ‘Cell-based’, which uses a set of pre-characterized and pre-verified logic cells, called Standard cell library. It contains a collection of components that are standardized at the logic or functional level, and consists of cells or macro-cells based on the unique layout. The economic and efficient accomplishment of an IC design depends heavily upon the choice of the library. In current SoC/ASIC designs, cell-bese design methodology is widely used. High-quality cell libraries are crucial for designing portable and high-performance devices. This paper presents a methodology

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for designing robust, low-area digital circuits which are incorporated as High density Standard Cell Library.

A. Significance of Standard cell libraries Independent blocks became too big and complex for a full-custom design, so there was a need to speed up the circuit and layout design processes. There was a shortage of specialized personnel capable of hand-crafting complex full-custom designed blocks; automation alleviated this problem. Advances in the typical manufacturing process included increasing the number of routing layers from one to two or three metal layers. This added further complexity to the full-custom layout design process for optimal results. Even in a full-custom design flow, the placement of more than 20 cells is easier when the building-block cells are implemented with predefined standards. The Standardization of cell interfaces is a concept that is implemented in a library. The solution was to simplify the circuit and layout design of large digital circuits by using predefined and characterized building blocks (cells). This High Density Library has been developed for 180nm process using UMC technology in Cadence 5.1.4.1. Table I lists the cell varieties of our library in logical function and drive strength. The driving strength range is wide from 1X to 64X and it advances the flexibility to various, load conditions, i.e. very small load to huge fan-out load, which is essential and indispensable requirement, especially in DSM technologies.

TABLE I

VARIATION IN FUNCTIONALITY AND DRIVE STRENGTH

FUNCTIONALITY	DRIVE STRENGTH
INV,BUFF	1X,2X,4X,8X,16X,32X,64X
NAND2,NAND3,NOR2,NOR3 AOI21,OAI21	1X,2X,4X
AND2,AND3,OR2,OR3	1X,2X,4X
MUX2,MUX4,XOR2	1X,2X
HAD1,FAD1	1X
D-FF,Dlatch	1X

In the first part of this paper, we present the design tech- nique employed for designing the standard cells. The layout techniques adopted for the physical design of logic cells has been explained in the second stage. Finally, to illustrate the efficacy of our standard cell library, we present the results as well as layouts of the logic cells. Conclusion and future work are presented in the last part of the paper.

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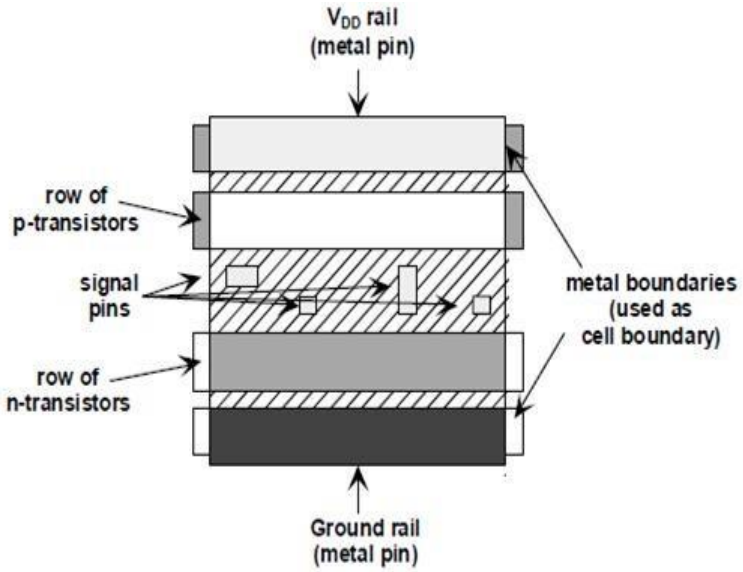
I. STANDARD CELL DESIGN

In this section, A table of Design Specifications has been presented, which has been used for developing the standard cells. The traditional device sizing methodology and the vari- ation driven design approach for various drive strength has been explained.

TABLE II

SPECIFICATIONS OF HIGH DENSITY STANDARD CELL LIBRARY

Parameters	High Density Library
Operating Frequency	500MHz
Number of tracks	07
Cell Height	5.04um
Output Rise time/Fall time	50ps ± 20 %
Supply Voltage	1.8V
Temperature Range	$-40^{\circ}C$ to $125^{\circ}C$
Standard Load (SL)	1.22fF
Drawn Gate Length	0.18 μm
Layers of Metal	1,2
Layout Grid	0.01μm
Cell Power/Ground Rail width	0.72 μm
Process Technology	UMC180
CAD Tool Cadence	5.1.4.1



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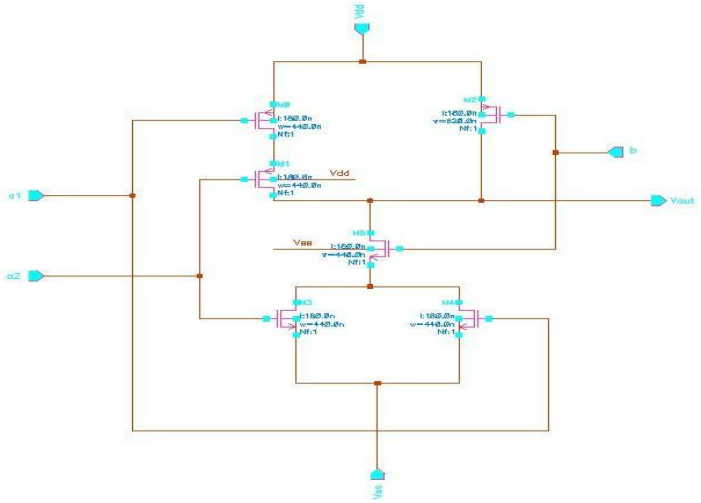

Fig.2 OR-And-Invert (OAI21) Schematic.

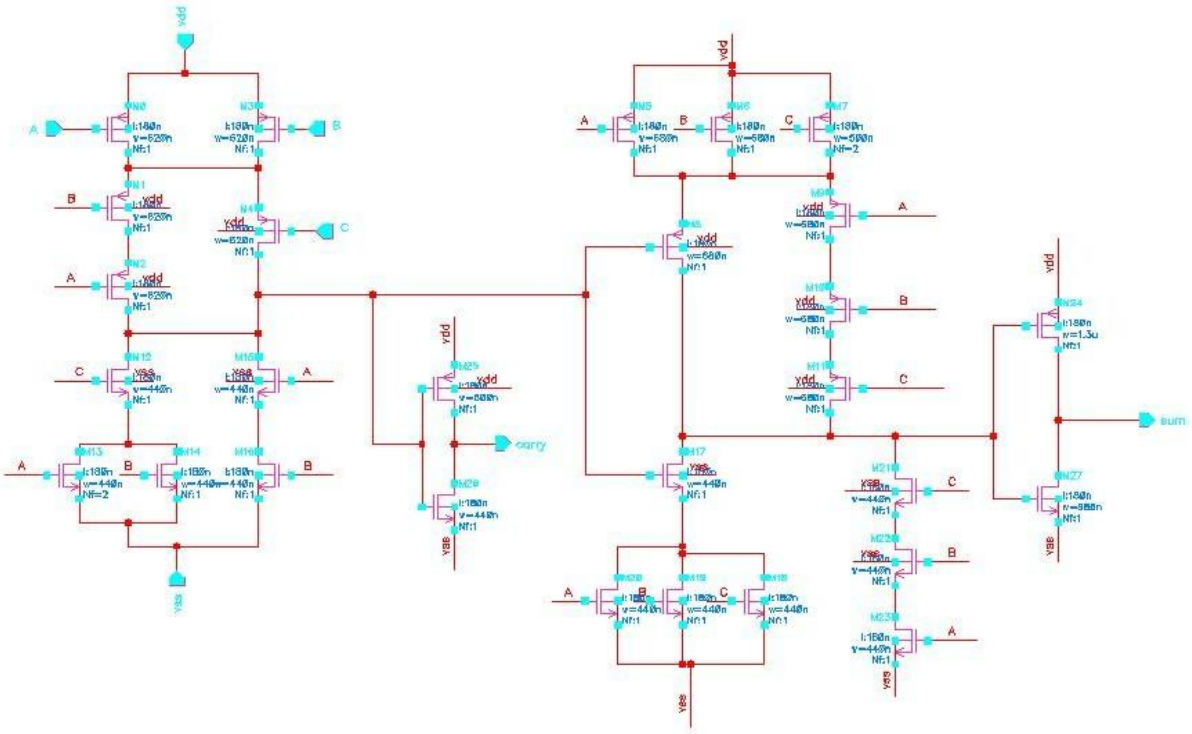

Fig.3 1 Bit Full Adder Schematic drive strengths are compared with respect to their ability to drive integer multiples of a standard load.

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The weakest cell is

Kn µnCox(W)n µn(W)n

A. Specifications

B. Design Methodes

C. For Symmetric Inverter where Kp is defind as;

$K_n = 1$ (1)

K_p

D. Single-Stage Gates

Higher drive strengths for static common CMOS gates (inverter, NAND,NOR) can be obtained by increasing both

Hence,(W)p ≈ 2.5(W)n

NMOS and PMOS sizes, once the cell size of their respective base cells has been fixed. The numeric label of the drive strength n, denotes the number of loads. For example a NAND2 4X drives a 4SL. Pull-up and pull-down networks are sized separately.

E. Multiple-Stage Gates

The cells based on transmission gate topologies(such as MUX and AOI) are classified as multiplestage gates in the library.The general strategy for sizing these gates is to make

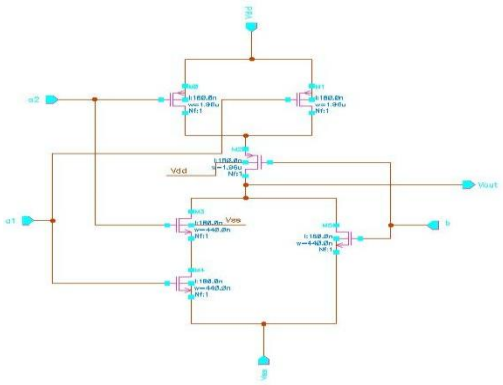

Fig.1 And-OR-Invert (AOI21) Schematic.

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C. Design Of Varying Drive Strength

The high density library provides several drive strength for each logic function, to be used in driving differently sized loads. Commonly used cells have more drive strength options available, while less common cells may need to be buffered in order to drive large loads. A traditional approach has been adopted for transistor sizing for different drive strengths, depending on the cell topology. Cells of different the output stage identical to the single-stage gate of the same drive strength. Transmission gates are not placed at the input or at the output stage of cells as the pass transistor logic is of little help when signal is of diminishing state.

II.PHYSICAL DESIGN OF STANDARD CELL

Cadence Virtuoso tool has been used for layout of Standard Cells. A template has been created to make the development of layouts easy. P-cells invoked have been flattened so as to achieve Design Rule Check(DRC) during the abutment of transistors. 1 DRC rule has maintained on all sides of the logic cells that, its DRC clean when abutted with other cells. Only M1 and M2 metal layers have been used for the cell layouts, leaving other metal layers for the auto routing tool used for higher

A.Special Considerations

For standard cell layout there is a set of special guidelines that has been followed. They are listed below:

- The sizes, shapes and locations of all geometries in layers pertinent to routing have been regularized. If a metal1 signal track inside the cell is 0.36µm wide, all other metal1 tracks inside the cell must also be 0.36µm wide.
- The general shape of the cell is as follows:

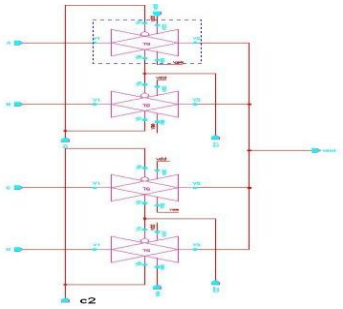

Fig.5 General shape of a standard core cell.

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• All metal tracks of the same layer (metal1, metal2, etc) for the same purpose (signal or power) are of same width.

• All power / ground pins have the same width and run in same directions all horizontal or all vertical.

• Attempts have been made to lay signal tracks of the same layer in the same direction.

• For any two adjacent signal track in the same metal layer running in the same direction, center-to-center pitch (defined below) are either same, or an integer multiply of a minimal pitch value (called routing pitch= 0.72µm).

• The routing pitch considered is via-to-via pitch (see figure 6.c). This will allow the routing tool to drop via where necessary. Line-to-line pitch or line-to-via pitch have been avoided, as the routing tool may fail since it is unable to drop a via when it is needed.

• Manhattan Routing technique has been followed where one metal layer is used for horizontal direction and another metal layer in vertical direction.

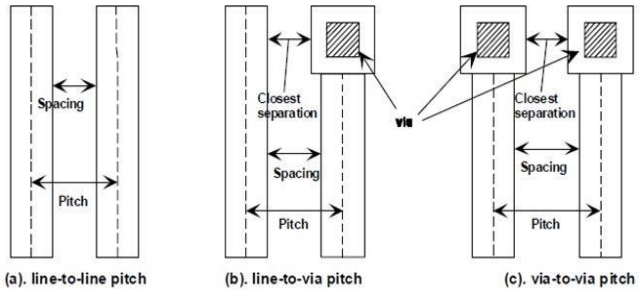

Fig.6 Definition of Routing Pitch

• All the MOSFETs are arranged, with their poly oriented in the same direction[10][9].

• The minimum width of PMOS and NMOS transistors assumed to be 440nm in-spite of the fact, the minimum transistor size for 180nm technology is 240nm. This is to avoid the dog bone structure(signal jogging in the active region) in the transistor as these signal joggs in the layers is difficult to manufacture using a mask layer. A mask layer with these small bends is difficult to manufacture, hence the transistor without the dog-bone structure is preferred.

• A minimum of two contacts for any metal to metal layer connectivity is added wherever possible[9]. This is done to improve the reliability of the design.

• Regardless of the number of metal layers provided by the technology, limilted number of metal layers are used for internal connections within the cells. Where ever possible, only metal1 has been used, so that all higher metal layer tracks are freely available for use by the routing tool.

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• Transistor fingering is done for large and critical tran- sistors [9][10]. The advantage with an even number of fingers is that the active capacitance is less, because the drain region is surrounded with gate poly instead of field.

• The technique of placing contacts for source and drain connections is to fit as many as we can using the min- imum design rule between two contacts. This guideline is most reliable and maximizes the performance of the transistor.

B.Creation of Template

A layout template is pre-requisite to a standard cell layout so as to maintain uniformity for all the cells. A template has been developed for this library pertaining to the specifications

.The standard cell library designed with 7 routing tracks. The tracks are so placed to achieve a DRC clean layout. Via to via spacing is assumed to be the minimum routing pitch. Hence in our case as higher metal layer used is Metal2, so Mvia2 to Mvia2 spacing is assumed to be minimum routing pitch. Therefore the routing pitch is 0.72µm . As the number of tracks used for high density cell library is 7 So, height of the standard cell is calculated to be= 0.72x7 =5.04µm Now as the cell height has been fixed, the maximum sizes of PMOS and NMOS that can be placed within this cell height have to be determined. as per the industry standards, the maximum PMOS/NMOS ratio is 60/40 percent of the cell height. Therefore the Maximum PMOS width = (60x5.04um)

/100 =3.024 µm the spacing between the N-well nd the active region of the PMOS = 0.43µm hence the width of the PMOS

= (3.024-.86)µm = 2.164µm 2.2µm similarly the Maximum width of NMOS transistor = (((40x5.04)/100)-.86) µm 1.12µm So the maximum PMOS and NMOS transistor sizes have been calculated to be as 2.2µm and 1.12µm respectively. Accordingly the N-well and the p-substrate regions for PMOS and NMOS respectively have been defined on the template. The transistor are placed in such a manner so as to have a DRC clean in th cas of a sea-of-gates arrangement is required 4 for an ASIC chip.

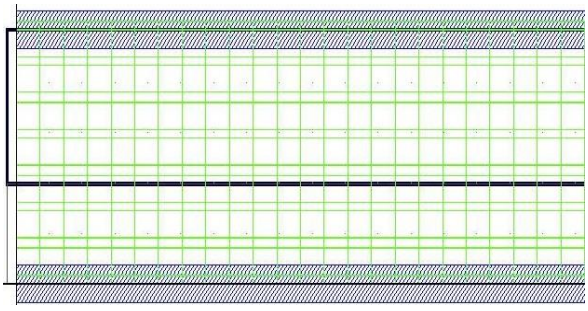

Fig.7 Template .

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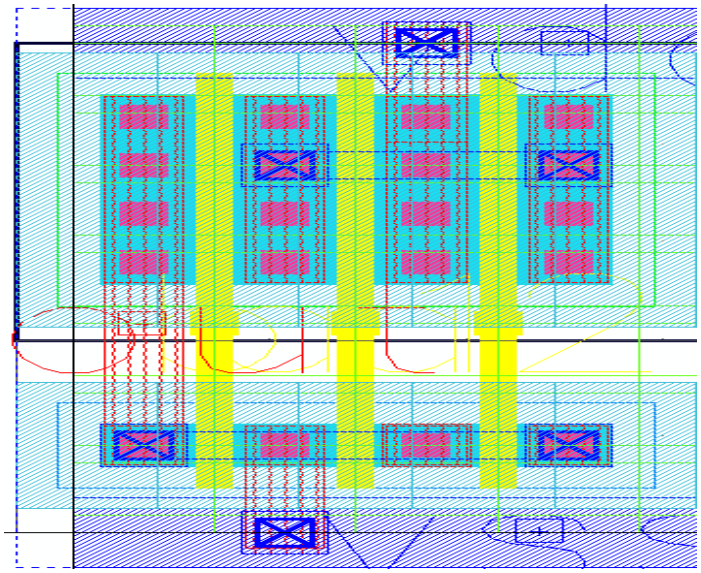

Fig.8 Layout of And-OR-Invert (AOI21).

III. SIMULATION RESULTS

We have mainly concentrated on the output slew rates, propagation delay, and the cell size of the standard cells developed for this high density libary. We have minimized the cell area and have tried to achive the timing constraints as per our specifications. The results and layouts of AOI, OAI,

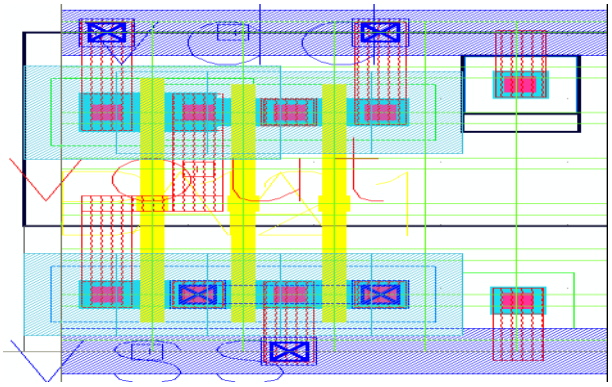

Fig.9 Layout of OR-And-Invert (OAI21).

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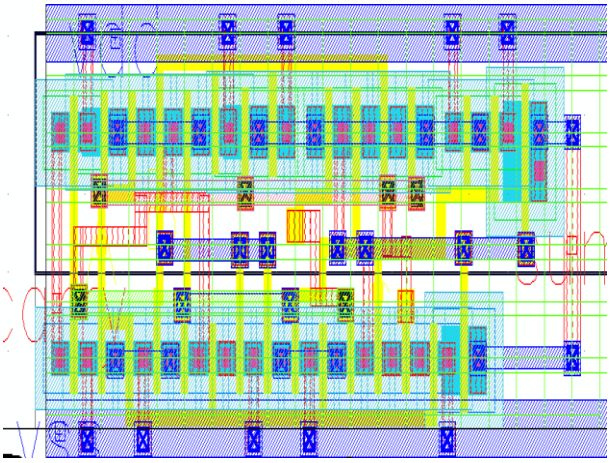

Fig.10 Layout of 1 Bit Full Adder.

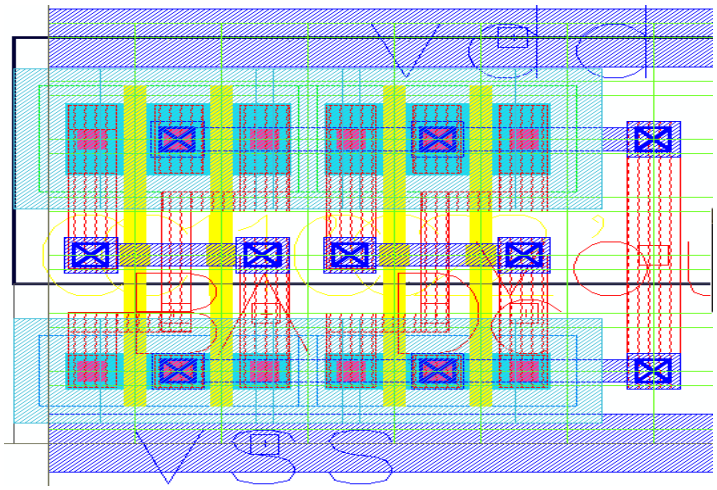

Fig.11 Layout of Mux4:1.

Full Adder and Mux cells for various drive strength have been presented. The simulations were carried out for the three even corners i.e. TT, SS and FF.

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IV. CONCLUSION AND FUTURE WORK

The design of High Density Standard cells is achieved which is operated for 500MHz, with a standard cell height of 5.04um with 7 tracks in the layout with 1.8V supply voltage, at a wide range of temperature.The power dissipation

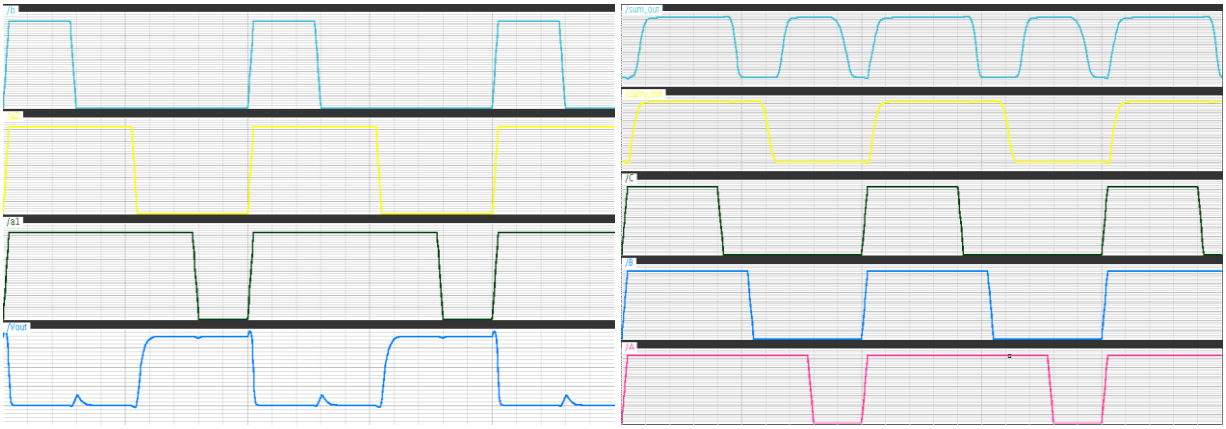

Fig.8 Waveform of And-OR-Invert.

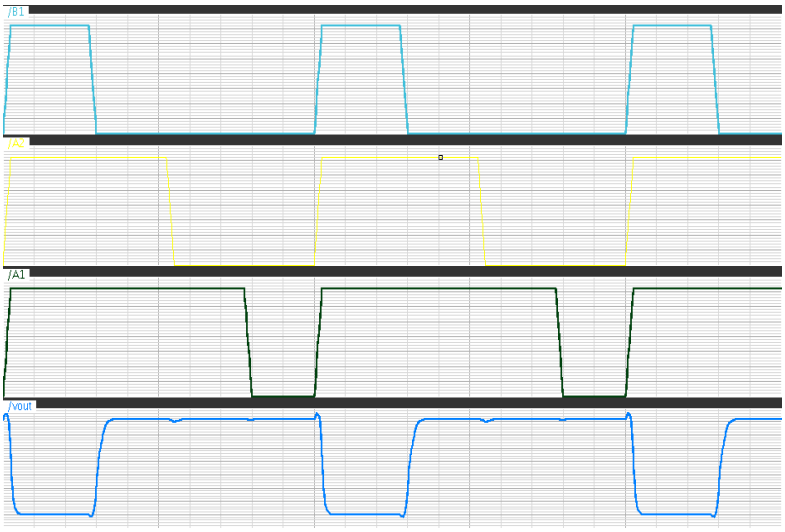

Fig.8 Waveform of OR-And-Invert.

of the Inverter64X circuit is 0.454mW. In this paper we implemented logic cells as per the specifications and achieve them with reduced cell area. This will involve trade of with the performance of the logic cells. A High Density Standard

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TABLE III

OUTPUT PARAMETERS OF AND-OR-INVERT (AOI21),1.8V, 27◦C

Parameters	Prelayout Simulations			Postlayout Simulations		
	tt	ss	ff	tt	ss	ff
tr(ps)	59.35	70.67	51.18	56.01	65.5	49.04
tf(ps)	19.29	23.5	17.02	19.41	23.29	17.35
delay(ps)	41.78	50.63	35.70	40.2	48.04	34.8

TABLE IV

OUTPUT PARAMETERS OF OR-AND-INVERT (OAI21),1.8V, 27◦C

Output	Parameters	Prelayout Simulations			Postlayout Simulations		
		tt	ss	ff	tt	ss	ff
Sum	**tr(ps)**	55.1	66.28	47.69	63.65	55.11	41.95
	tf(ps)	48.48	47.43	35.26	47.16	75.08	56.2
	delay(ps)	126	168	102.6	152	201	123.6
Carry	**tr(ps)**	55.05	66.24	47.13	63.03	76.55	53.69
	tf(ps)	55.48	66.07	51.01	73.64	85.05	65.04
	delay(ps)	210.7	203.1	217.0	86.96	109.4	73.62

Fig.8 Waveform of 1 Bit Full Adder.

Output	Parameters	Prelayout Simulations			Postlayout Simulations		
		tt	ss	ff	tt	ss	ff
Sum	**tr(ps)**	55.1	66.28	47.69	63.65	55.11	41.95
	tf(ps)	48.48	47.43	35.26	47.16	75.08	56.2
	delay(ps)	126	168	102.6	152	201	123.6
Carry	**tr(ps)**	55.05	66.24	47.13	63.03	76.55	53.69
	tf(ps)	55.48	66.07	51.01	73.64	85.05	65.04
	delay(ps)	210.7	203.1	217.0	86.96	109.4	73.62

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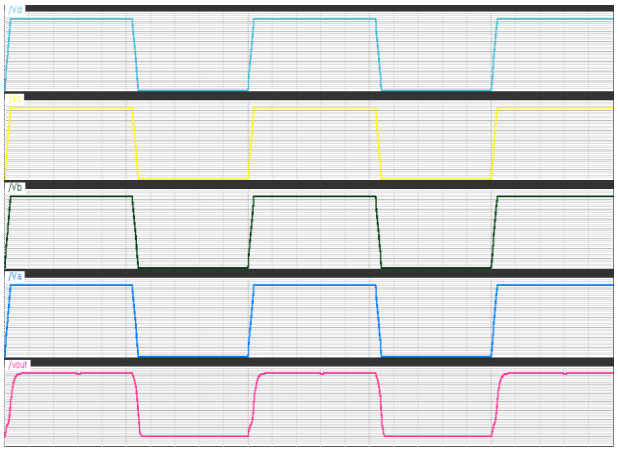

Fig.9 Waveform of Mux4:1.

TABLE VI

OUTPUT PARAMETERS OF MUX 4:1,1.8V, 27◦C

Parameters	Prelayout Simulations			Postlayout Simulations		
	tt	ss	ff	tt	ss	ff
tr(ps)	53.59	63.98	46.42	58.6	70.46	50.55
tf(ps)	27.2	34.51	32.34	30.49	38.86	26.12
delay(ps)	37.30	45.27	32.4	40.4	49.02	34.94

Parameters	Prelayout Simulations			Postlayout Simulations		
	tt	ss	ff	tt	ss	ff
tr(ps)	45.56	49.14	46.98	48.13	56.6	47.22
tf(ps)	32.03	36.02	29.9	34.63	39.54	32.21
delay(ps)	24.69	28.8	21.82	26.28	30.79	23.31

Cell Library is implemented successfully. By calculations and results we found that High Density Standard Cell library is improved and cell sizes for the Standard cells are reduced. The future work may include the automation of the standard cells implemented for different conditions. This is in turn could be sent to a fabrication for verifying results.

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