



ONLINE SURFACE ROUGHNESS CALCULATION USING MACHINE VISION AND IMAGE PROCESSING

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Abstract

Machine vision has advanced to become a widely used automation technology, allowing computers to take over human vision in high-speed and precise production methods. Images captured by contemporary cameras sometimes suffer from contamination caused by many sources of noise, as well as a decrease in intensity. In many situations, the specific kind of noise and the lighting conditions are also unknown beforehand. This study presents the construction of an image operator that utilises an evolutionary strategy for light enhancement and noise filtering. The suggested structure has an advantage in that it is derived from basic building blocks. The setup of evolvable hardware (EHW) use the programmable Xilinx Virtex2 FPGA xc4000 architecture. The performance of the proposed image operator is evaluated by applying it to pictures of machined component surfaces captured using vision systems with a linearly decreasing intensity. Next, the improved picture resulting from evolution is analysed, and a correlation between the characteristics of the surface image and the true surface roughness is determined by regression analysis. In comparison to the stylus approach, the computer vision system that has been developed is a valuable technique for detecting surface roughness in computer integrated manufacturing processes (CIM). It offers quicker results, reduced environmental noise, and is more cost-effective.

Keywords: Evolvable Hardware, Neural Network, Surface Roughness

1. Introduction

Evolvable systems, also known as EHW, are hardware units that use software reconfigurable logic devices like FPGA and PLD. These units have the ability to alter their design via genetic learning. In order to create traditional hardware, it is essential to prearrange all the specifications for the hardware functions beforehand. On the other hand, EHW has the ability to adapt and improve its performance without the need for precise instructions. The fundamental concept of EHW is using the architectural bits of a reconfigurable device as a chromosome for a genetic algorithm (GA), which aims to discover an ideal hardware structure. In the field of digital image processing, there are various applications that utilise evolutionary computation. These applications include the use of genetic algorithms to segment medical resonance imaging scans, a genetic programme that detects edges in one-dimensional signals, the evolution of genetic programmes to detect edges in petrographic images, and the evolution of spatial masks to detect edges in grayscale images. This work introduces an evolvable hardware architecture designed specifically for achieving high-performance picture noise filtering on a bespoke Xilinx Virtex FPGA xcv1000. The system also includes a configurable local interconnect hierarchy. Once the photos are processed utilising the EHW system, the resulting high-quality photographs of surfaces are used to assess the surface finish.

2. Evolvable Hardware System

The EHW architecture may be categorised into functional and gate level [2] and is seen in Figure 1 and 2. In gate level electronic hardware (EHW), the architectural components of programmable logic devices (PLDs) are regarded as genetic algorithm (GA) chromosomes. The architectural components may be obtained by downloading them onto Programmable Logic Devices (PLDs). Downloading may be done either during or after the learning process.

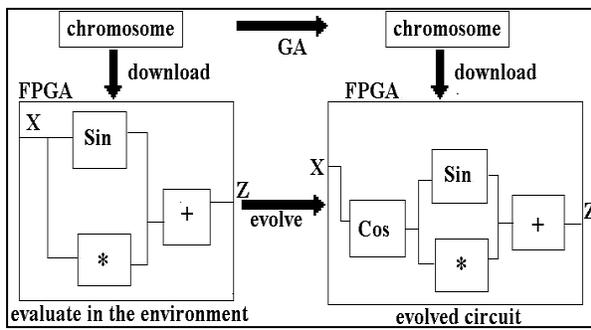


Figure 1 Functional level evolution

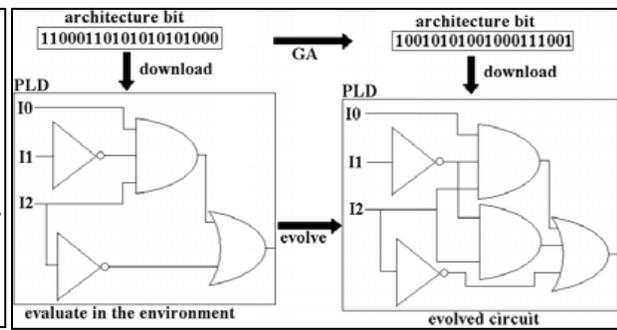


Figure 2 Gate level evolution

3. Measurement of the Surface Image of Work Piece

Figure 3 displays a schematic representation of the machine vision system used for examining surface roughness in milling operations. The system comprises a light source and a CCD camera with a resolution of 512×640 to collect surface images. These images are then sent to the EHW system for further analysis and processing.

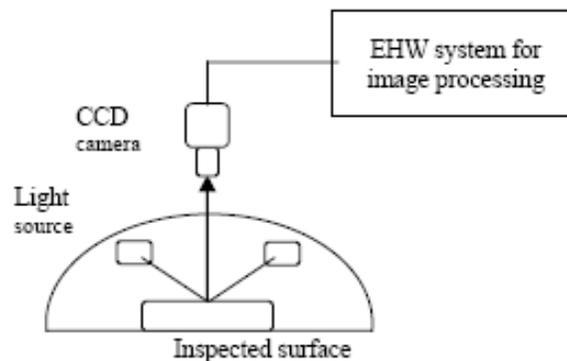


Figure 3 Machine vision system

To assess surface roughness under various cutting circumstances, a series of cutting experiments were conducted utilising a Milling machine equipped with a carbide tool, while working on mild



steel bars. Experiments were conducted to collect data on various cutting parameters, including feed rate, cutting speed, and depth of cut. The roughness of the machined surface was determined using a profile metre (Surfcorder SE1200) with a sample length of 8mm and a measuring speed of 0.5mm/s. The surface roughness metric used in this investigation is the mean surface roughness (Ra). The term refers to the mean value of the absolute heights of roughness irregularities assessed from the average value.

4. Reconfigurable Architecture

Figure 4 displays the virtual reconfiguration chip (VRC) of the EHW unit. In this study, it is assumed that every processing element (PE) except for the first stage may accept inputs from any of the preceding two stages. There were a total of 25 processing elements (PEs) employed in the virtual reality controller (VRC). The genetic unit is designed to choose the optimal chromosome, which is then used to determine the initial configuration of the VRC. Table 1 provides a list of 16 distinct tasks that each PE is capable of doing.

Table 1 Function codes

Code	Function	Code	Function
F0: 0000	$X \gg 1$	F8 : 1000	$(X+Y+1) \gg 1$
F1: 0001	$X \gg 2$	F9 :1001	$X \& 0x0F$
F2: 0010	$\sim X$	F10: 1010	$X \& 0xF0$
F3: 0011	$X \& Y$	F11: 1011	$X 0x0F$
F4: 0100	$X Y$	F12: 1100	$X 0x F0$
F5: 0101	$X \wedge Y$	F13: 1101	$(X\&0x0F) (Y\&0xF0)$
F6: 0110	$X + Y$	F14: 1110	$(X\&0x0F) \wedge (Y\&0xF0)$
F7: 0111	$(X+Y) \gg 1$	F15: 1111	$(X\&0x0F) \& (Y\&0xF0)$

The circuit's logical configuration is determined by a collection of 25 inter triplets, with each triplet corresponding to one of the 25 processing elements (PEs) in the reconfigurable design. The first two values in each triplet indicate the input sources for the processing element (cfg1 and cfg2), while the third integer (cfg3) specifies the index of the function (as shown in Table 1) to be executed by the processing element.

5. Evolution of Chip

Figure 5 illustrates the planned EHW system. The configuration word provides information on the interconnection between the processing elements (PEs) of the virtual routing controller (VRC) and the specific functional activities carried out inside each PE.

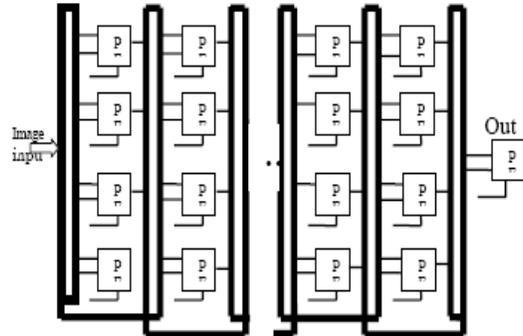


Figure 4 Reconfigurable architecture

The inputs for each processing element (PE) are selected from the outputs of the two preceding columns using a multiplexer. Both $cfg1$ and $cfg2$ are limited by the constraint that they must not exceed the number of inputs of the multiplexer. The $cfg3$ input represents the number of functions in storage using binary notation.

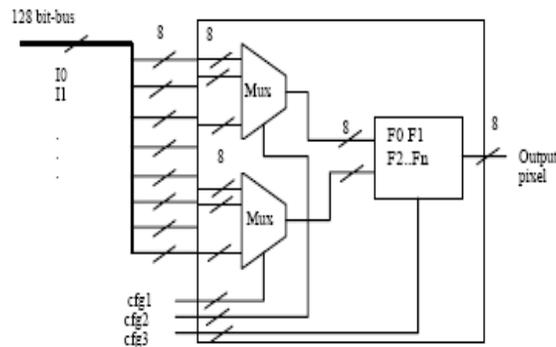


Figure 5 Architecture of a single PE [output = $F\{\text{mux}(cfg1), \text{mux}(cfg2), cfg3\}$]

6. Details of High Speed Image

Processing Card

The video processing card being suggested is connected to the PCI bus and serves as a cost-effective platform for creating video and multimedia applications. The card is equipped with an integrated high-speed video analog-to-digital converter (ADC) and digital-to-analog converter (DAC). The board facilitates the real-time processing of video data from various components. The on-board SRAM and Flash memory are used for data storage, namely for storing the configuration bits of the VRC. The code for the Genetic processor is stored in the power PC that is included on the board. The card that has been created may function independently as a video processing board. The board uses the XCZVP30 FPGA processor. The card has five completely separate sets of IMX16SRAM and three completely separate sets of 512K x 16 flash PROM. The sampling rate is 30 million samples per second (MSPS). Figure 6 displays the prototype of the high-speed card.



Figure 6 High speed Image Processing Card

Experimental Results

The CCD camera captures surface pictures of the specimens, which are then inputted into the EHW Chip. A configuration word is chosen to mitigate the impact of inadequate lighting and noise. Preprocessing is conducted to improve the quality of pictures. The chip processes input pictures 'I' of resolution $m \times n$ by extracting the edges and replacing the original poor quality image with an output image 'O'. In the trials, the starting population size is fixed at 16. Each chromosome undergoes evolution with a crossover rate of 0.9 and a mutation rate of 0.01. Figure 7 displays the photographs that have been affected by noise, whereas Figure 8 exhibits the preprocessed images achieved via the use of the EHW system. The two pictures seen in Figure 7 are the unprocessed photographs acquired using a vision system. The evolvable hardware chip unit improves the picture quality by 62.5%. The surface roughness values acquired using the stylus method, together with the parameters feed, depth of cut (doc), and spindle speed, are stated. The surface finish values achieved by employing the evolvable hardware system on the milled surface are compared with other ways and shown in Table 2.



Figure 7 Images with noise

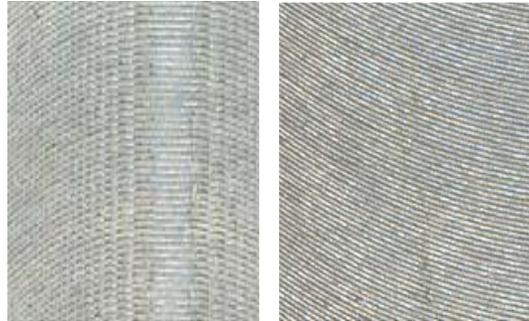


Figure 8 Images without noise

Table 2 Surface Finish Values

S.N	Feed (mm/rev)	Doc (mm)	Speed (m/min)	R _a (Stylus) (μm)	R _a Reg. Analysis (μm)	R _a EHW (μm)
1	150	0.5	123	3.05	3.23	3.12
2	150	0.8	123	3.19	2.61	3.18
3	150	0.5	153	5.35	6.05	5.58
4	200	0.5	123	5.62	6.13	5.34
5	200	0.8	123	3.75	3.38	3.48
6	200	0.5	153	2.94	1.95	2.89

7. Conclusion

This work introduces a genetic algorithm-based EHW chip for analysing the surface roughness of components produced during milling. The pictures are preprocessed to eliminate noise before analysis. The correlation achieved via regression analysis after upgrading the quality of the surfaces using the EHW technique was superior to that obtained without image enhancement. The experimental findings unambiguously demonstrate that the suggested approach is capable of assessing the roughness of the machined surfaces. The next research will concentrate on using an artificial neural network (ANN) to forecast the surface roughness by employing picture information as input.

8. References

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