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CALCULATING SURFACE ROUGHNESS ONLINE USING MV AND IMAGE PROCESSING

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Abstract

Machine vision has advanced to become a widely used automation technology, allowing computers to take over human vision in high-speed and precise production methods. Images captured by contemporary cameras sometimes suffer from contamination caused by many sources of noise, as well as a decrease in intensity. Additionally, the specific kind of noise and the lighting conditions are typically not known in advance. This study presents the creation of an image operator that utilises an evolutionary strategy to boost lighting and filter noise. The suggested structure has an advantage in that it is derived from basic elements. The evolvable hardware (EHW) setup uses the reconfigurable Xilinx Virtex2 FPGA xc4000 architecture. The performance of the proposed image operator is evaluated by applying it to pictures of machined component surfaces captured using vision systems with a linearly decreasing intensity. The improved picture resulting from the process of evolution is further analysed, and a correlation between the characteristics of the surface image and the real roughness of the surface is determined by regression analysis. In comparison to the stylus approach, the computer vision system that has been developed is a valuable technique for detecting surface roughness in computer integrated manufacturing processes (CIM). It offers quicker results, less environmental noise, and a cheaper cost.

Keywords: Evolvable Hardware, Neural Network, Surface Roughness

1. Introduction

Evolvable systems, also known as EHW, are hardware units that use software reconfigurable logic devices like FPGA and PLD. These units have the ability to modify their design via genetic learning. In order to develop traditional hardware, it is important to predefine all the specifications for the hardware functionalities. On the other hand, EHW is capable of reconfiguring itself without explicit instructions in order to enhance its performance. The fundamental concept of EHW is using the architectural bits of a reconfigurable device as a chromosome for a Genetic Algorithm (GA) that aims to find an ideal hardware structure. In the field of digital image processing, there is a wide variety of applications that utilise evolutionary computation. These applications include the use of genetic algorithms to segment medical resonance imaging scans, a genetic programme that detects edges in one-dimensional signals, the evolution of genetic programmes to detect edges in petrographic images, and the evolution of spatial masks to detect edges in grey scale images. This work introduces an evolvable hardware architecture designed specifically for achieving high-performance picture noise filtering on a bespoke Xilinx Virtex FPGA xcv1000. The system also includes a configurable local interconnect hierarchy. Upon applying the EHW system to the originally captured photos, the resulting photographs of surfaces with enhanced quality are used for the assessment of surface finish.

2. Evolvable Hardware System

The EHW architecture may be categorised into functional and gate level [2] and is seen in Figure 1 and 2. In gate level electronic hardware (EHW), the architectural bits of programmable logic devices (PLDs) are considered as genetic algorithm (GA) chromosomes. The architectural components may be obtained by downloading them onto Programmable Logic Devices (PLDs). Downloading may be done either during or after the learning process.

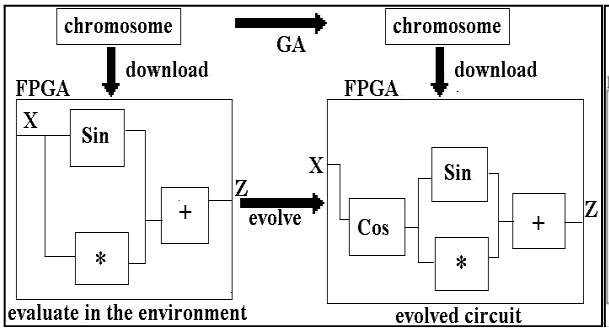

Figure 1 Functional level evolution

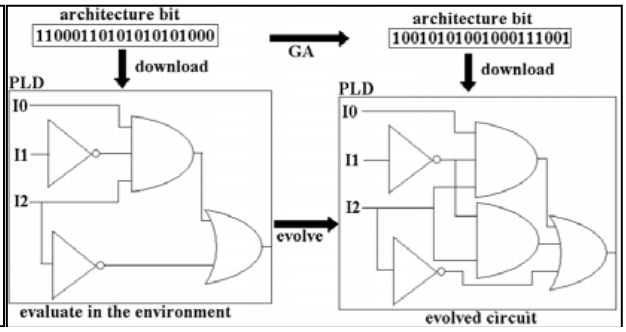

Figure 2 Gate level evolution

3. Measurement of the Surface Image of Work Piece

Figure 3 displays a schematic design of the machine vision system used to examine surface roughness during milling operations. The system comprises a light source and a CCD camera with a resolution of 512 × 640 to collect surface images. These images are then sent to the EHW system for further analysis and processing.

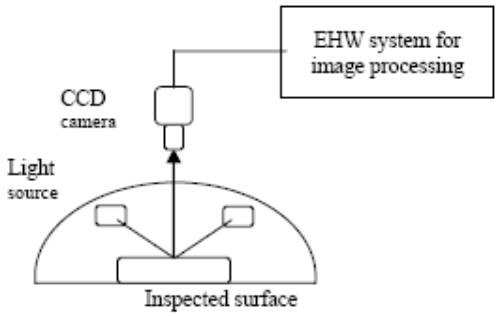

Figure 3 Machine vision system

To assess surface roughness under various cutting circumstances, a series of cutting experiments were conducted utilising a Milling machine equipped with a carbide tool, while working on mild steel bars. Experiments were conducted to collect data on various cutting parameters, including feed rate, cutting speed, and depth of cut. The surface roughness of the machined surface was determined using a profile metre called Surfcorder SE1200. The measurements were taken across a length of 8mm and at a speed of 0.5mm/s. The surface roughness metric used in this investigation is the mean surface roughness (Ra). The term refers to the mean value of the absolute heights of roughness irregularities assessed from the average value.

4. Reconfigurable Architecture

Figure 4 displays the virtual reconfiguration chip (VRC) of the EHW unit. In this study, it is assumed that every processing element (PE) except for the first stage may accept inputs from any of the preceding two stages. There were a total of 25 processing elements (PEs) employed in the virtual reality controller (VRC). The genetic unit is designed to choose the optimal chromosome, which is then used to determine the initial configuration of the VRC. Table 1 provides a list of 16 distinct functions that each PE may handle.

Table 1 Function codes

Code	Function	Code	Function
F0: 0000	X >> 1	F8 : 1000	(X+Y+1) >> 1
F1: 0001	X >> 2	F9 :1001	X & 0x0F
F2: 0010	~ X	F10: 1010	X & 0xF0
F3: 0011	X & Y	F11: 1011	X | 0x0F
F4: 0100	X | Y	F12: 1100	X | 0x F0
F5: 0101	X ^ Y	F13: 1101	(X&0x0F) | (Y&0xF0)
F6: 0110	X + Y	F14: 1110	(X&0x0F) ^ (Y&0xF0)
F7: 0111	(X+Y) >> 1	F15: 1111	(X&0x0F) & (Y&0xF0)

The circuit's logical configuration is determined by a collection of 25 inter triplets, with each triplet corresponding to one of the 25 processing elements (PEs) in the reconfigurable design. The first two numbers of each triplet denote the inputs to the processing element (PE) as cfg1 and cfg2, while the third integer of the triplet (cfg3) indicates the index of the function (as shown in Table 1) to be executed by the PE.

5. Evolution of Chip

Figure 5 illustrates the planned EHW system. The configuration word includes specific information about the connectivity among the processing elements (PEs) of the virtual reality controller (VRC) and the functional activities executed inside each PE.

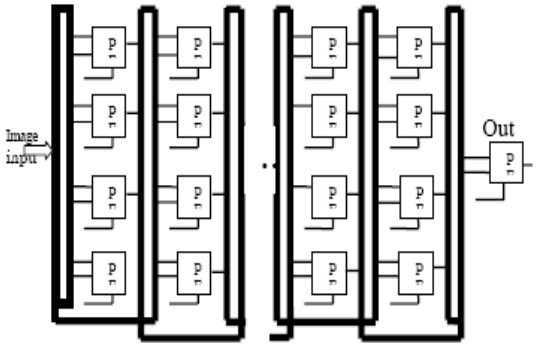

Figure 4 Reconfigurable architecture

The multiplexer inputs for each processing element (PE) are selected from the outputs of the preceding two columns. Both cfg1 and cfg2 are limited by the constraint that they must not exceed the number of inputs of the multiplexer. The cfg3 input represents the numerical value of the total number of functions stored, expressed in binary form.

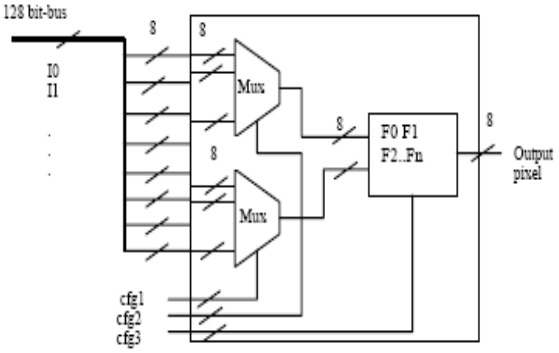

Figure 5 Architecture of a single PE [output = F {mux(cfg1), mux(cfg2), cfg3}]

6. Information of High Speed Image

Processing Card

The video processing card under consideration is connected to the PCI bus and serves as a cost-effective platform for creating video and multimedia applications. The card is equipped with an integrated high-

speed video analog-to-digital converter (ADC) and digital-to-analog converter (DAC). The board facilitates the real-time processing of video data from various components. The on-board SRAM and Flash memory are used for data storage, namely for storing the configuration bits of the VRC. The code for the Genetic processor is stored in the power PC that is included on the board. The card that has been created may function independently as a video processing board. The board uses the XCZVP30 FPGA processor. The card has five separate and autonomous banks of IMX16SRAM and three separate and autonomous banks of 512K x 16 flash PROM. The sampling rate is 30 million samples per second (MSPS). Figure 6 displays the prototype of the high-speed card.

Figure 6 High speed Image Processing Card

Experimental Results

The CCD camera captures surface pictures of the specimens, which are then inputted into the EHW Chip. A configuration word is chosen to mitigate the impact of inadequate lighting and noise. Preprocessing is conducted to improve the quality of pictures. The chip processes input pictures 'I' of resolution m x n by extracting the edges and replacing the original poor quality image with an output image 'O'. In the trials, the starting population size is fixed at 16. Each chromosome undergoes evolution with a crossover rate of 0.9 and a mutation rate of 0.01. Figure 7 displays the photographs that have been affected by noise, whereas Figure 8 exhibits the preprocessed images using the EHW technique. The two pictures shown in Figure 7 are the unprocessed images acquired via the use of a vision system. The evolvable hardware chip unit improves the picture quality by 62.5%. The surface roughness values produced by the stylus method, considering the parameters feed, depth of cut (doc), and spindle speed, are shown in Table 2. Additionally, the surface finish values achieved utilising the evolvable hardware system on the milled surface are compared with other methods.

Figure 7 Images with noise

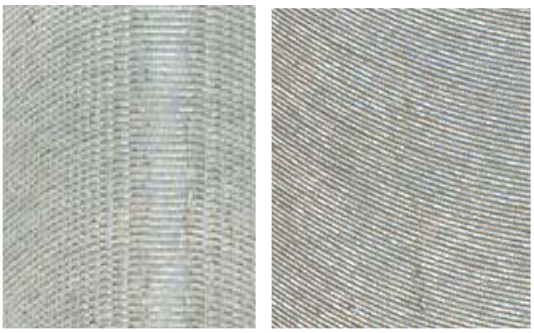

Figure 8 Images without noise

Table 2 Surface Finish Values

S.N	Feed (mm/rev)	Doc (mm)	Speed (m/min)	R_a (Stylus) (µm)	R_a Reg. Analysis (µm)	R_a EHW (µm)
1	150	0.5	123	3.05	3.23	3.12
2	150	0.8	123	3.19	2.61	3.18
3	150	0.5	153	5.35	6.05	5.58
4	200	0.5	123	5.62	6.13	5.34
5	200	0.8	123	3.75	3.38	3.48
6	200	0.5	153	2.94	1.95	2.89

7. Conclusion

This work introduces a genetic algorithm-based EHW chip for analysing the surface roughness of components produced during milling. The pictures are preprocessed to eliminate noise before analysis. The correlation achieved by regression analysis, after the enhancement of surface quality utilising the EHW method, was superior to that obtained without image enhancement. The experimental findings unambiguously demonstrate that the suggested approach is capable of assessing the roughness of the machined surfaces. The next research will concentrate on using an artificial neural network (ANN) to forecast the surface roughness by employing picture information as input.

8. References

[1]. P. Layzell, "A new research tool for intrinsic hardware evolution", Proc. 2nd International Conference on Evolvable Systems (ICES'98), 47-56, Springer-Verlag, 1998
[2]. Vandenberg et al., "Digital image processing techniques, fractal dimensionality and scale-space applied to surface roughness", Wear, 159, 1992, 17-30
[3]. Poli, "Genetic programming for image analysis", Genetic Programming: Proceedings of the first Annual Conference, 1996, 363-368
[4]. B. Ross, F. Feutan and D. Yashkir, "Edge detection of petrigraphic images using genetic programming brock computer science technical reports", Brock University, Ontario, Canada CS-00-01, 2000
[5]. C. Harris and B. Buxton, "Evolving edge detectors", Research Note RN/96/3(1996), University College London, 1996, 356-379
[6]. Yin S, Nguyen D, Chen F, Tang Q, Duc LA. Application of compressed air in the online monitoring of surface roughness and grinding wheel wear when grinding Ti-6Al-4V titanium alloy. The International Journal of Advanced Manufacturing Technology. 2019 Apr 6;101:1315-31.
[7]. Joshi K, Patil B. Prediction of surface roughness by machine vision using principal components based regression analysis. Procedia Computer Science. 2020 Jan 1;167:382-91.
[8]. John JG, Arunachalam N. Illumination compensated images for surface roughness evaluation using machine vision in grinding process. Procedia Manufacturing. 2019 Jan 1;34:969-77.
[9]. Patel DR, Kiran MB, Vakharia V. Modeling and prediction of surface roughness using multiple regressions: A noncontact approach. Engineering Reports. 2020 Feb;2(2):e12119.

[10]. Akhil V, Raghav G, Arunachalam N, Srinivas DS. Image data-based surface texture characterization and prediction using machine learning approaches for additive manufacturing. Journal of Computing and Information Science in Engineering. 2020 Apr 1;20(2):021010.